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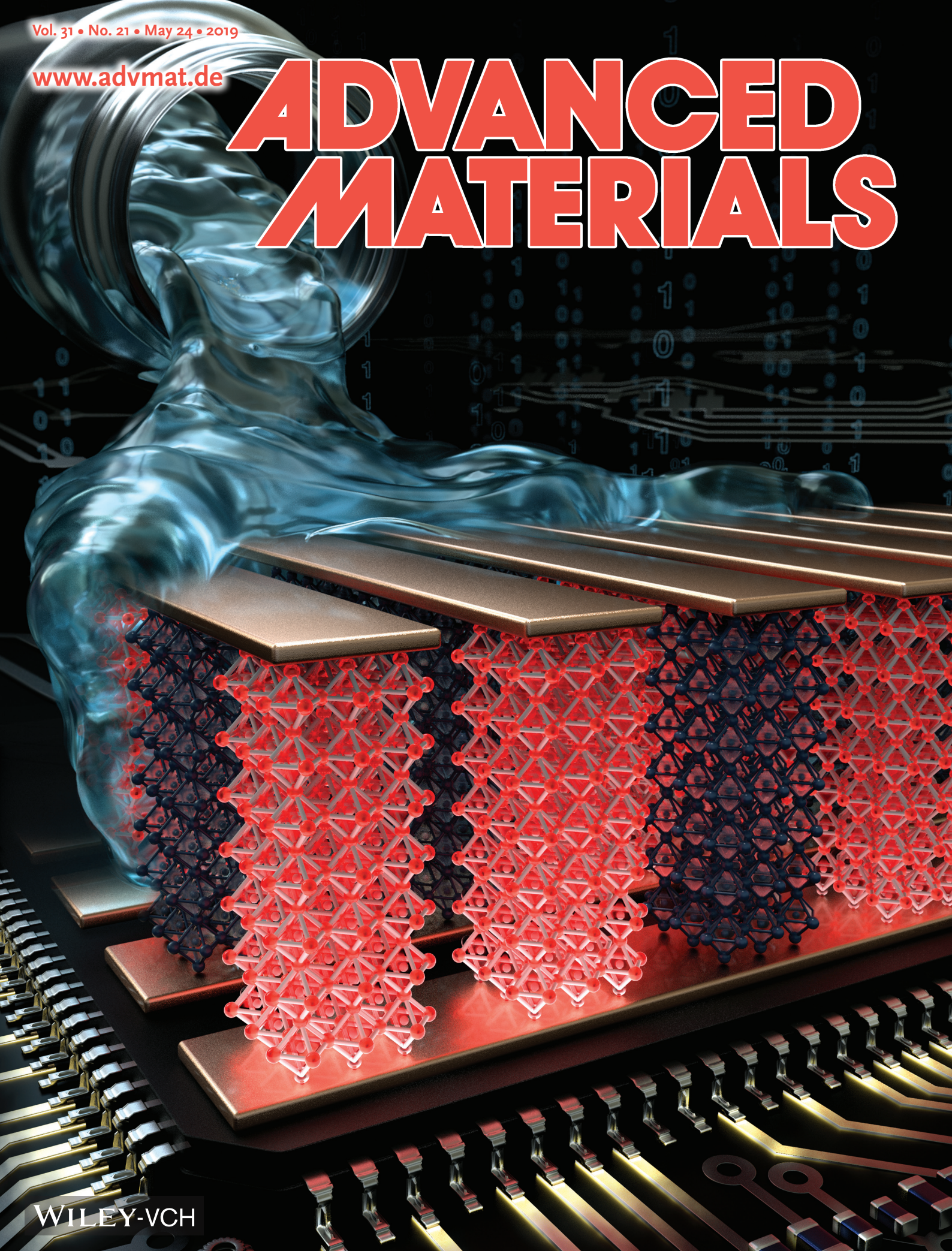

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High-Performance Solution-Processed Organo-Metal Halide Perovskite Unipolar Resistive Memory Devices in a Cross-Bar Array Structure

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Resistive random access memories can potentially open a niche area in memory technology applications by combining the advantages of the long endurance of dynamic random-access memory and the long retention time of flash memories. Recently, resistive memory devices based on organo-metal halide perovskite materials have demonstrated outstanding memory properties, such as a low-voltage operation and a high ON/OFF ratio; such properties are essential requirements for low power consumption in developing practical memory devices. In this study, a nonhalide lead source is employed to deposit perovskite films via a simple single-step spin-coating method for fabricating unipolar resistive memory devices in a cross-bar array architecture. These unipolar perovskite memory devices achieve a high ON/OFF ratio up to 10^8 with a relatively low operation voltage, a large endurance, and long retention times. The high-yield device fabrication based on the solution-process demonstrated here will be a step toward achieving low-cost and high-density practical perovskite memory devices.

Resistive random access-memory (RRAM) has emerged as a promising candidate as the next-generation memory technology because of their advantages such as nonvolatility, low operational energy, and simple operation principles based on resistive switching effect.[1,2] Moreover, a metal–insulator–metal structure commonly used for an RRAM cell has a scaling potential in the form of a cross-bar architecture, in which memory cells are sandwiched between a set of parallel bottom electrode lines (word lines) running perpendicular to top electrode counterparts (bit lines).[3,4] The cross-bar geometry enables a highly integrated RRAM architecture with the minimum cell size defined by $4F^2$ (F = minimum feature size[3]) and has been even projected to overcome the scaling limit of current silicon-based Flash memory technologies.[4]

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During the last decade, RRAM devices based on solution-processed materials have been extensively explored owing to their easy and low-cost fabrication processes. In particular, the performance of memory devices made with solution-processed organic and organic–inorganic hybrid materials[5–9] has improved significantly due to a concerted effort of creative material designs and an active pursuit of the resistive switching mechanism governing the memory operation.

Recently, organo-metal halide perovskite materials with ABX_3 structure, where A is an organic cation, B is a metal ion, and X is a halide anion, have demonstrated their excellent material properties for the devices applications in solar cell and light-emitting devices,[10–12] as well as memory devices. In particular, resistive memory devices based on perovskite materials have shown promising device performances, such as a low-voltage operation, long retention time, and high ON/OFF ratio.[13–17] One of the well-established perovskite materials is methylammonium lead iodide ($MAPbI_3$) for which various solution-processing methods for thin-film deposition have been developed for high-efficiency optoelectronic devices, including single-step spin-coating, sequential deposition,[18–20] and solvent-engineering techniques.[10,21,22] A widely used technique in perovskite film deposition for RRAM fabrication is the solvent-engineering method (or known as "solvent-dropping"), in which a fast deposition–crystallization[21] is induced by dropping a solvent during the spin-coating of a solution mixture of methylammonium iodide (MAI) and lead iodide (PbI_2).[14,15,17,23,24] Although this method has been used to produce a denser and more uniform perovskite film than the conventional single-step spin-coating method or the sequential deposition method, the film quality is extremely sensitive to the solvent-dropping conditions such as the type, amount, the time, and the position of displacement of the solvent;[21,22] this sensitivity potentially limits its applicability for large-scale film deposition. Moreover, Zhang et al.[25] discovered that the lead-containing precursor played an important role in the perovskite crystal growth and that the use of $PbAc_2$ in a simple single-step spin-coating method achieved a highly uniform and dense perovskite film without any additional solvent-engineering.

Here, we studied perovskite RRAM devices in a cross-bar array structure with solution-processed $MAPbI_3$ memory elements prepared from $PbAc_2$ by a single-step spin-coating method. The characteristics of memory devices made from this deposition method showed a desirable performance, with a high ON/OFF ratio, good retention time and endurance cycles, and the low operation voltage. In addition, the uniform perovskite film produced from the $PbAc_2$ precursor achieved high-yield (up to 94%) memory devices in an 8×8 cross-bar array structure with uniform memory cell characteristics. Furthermore, to avoid a cross-talk interference problem among the memory cells in the 8×8 cross-bar array structure, we utilized one diode–one resistor (1D–1R) scheme using our perovskite RRAM devices exhibiting unipolar resistive switching behaviors.

The perovskite memory devices focused in this study were fabricated with top and bottom Au electrodes in a device structure of $Au/MAPbI_3/Au$. The $MAPbI_3$ perovskite film was deposited via a simple one-step spin-coating method with a nonhalide lead precursor, $PbAc_2$ mixed with MAI. While annealing the film after the spin-coating, perovskite crystals form according to the chemical reaction, $3MAI + PbAc_2 = MAPbI_3 + 2MAAc$ (see **Figure 1**a,b), where MAAc refers to methylammonium acetate. This method induces a rapid crystal growth that results in a nearly pinhole-free ultrasmooth film formation.[25,26] The higher film quality compared to that of films made from lead halide precursors (i.e.,

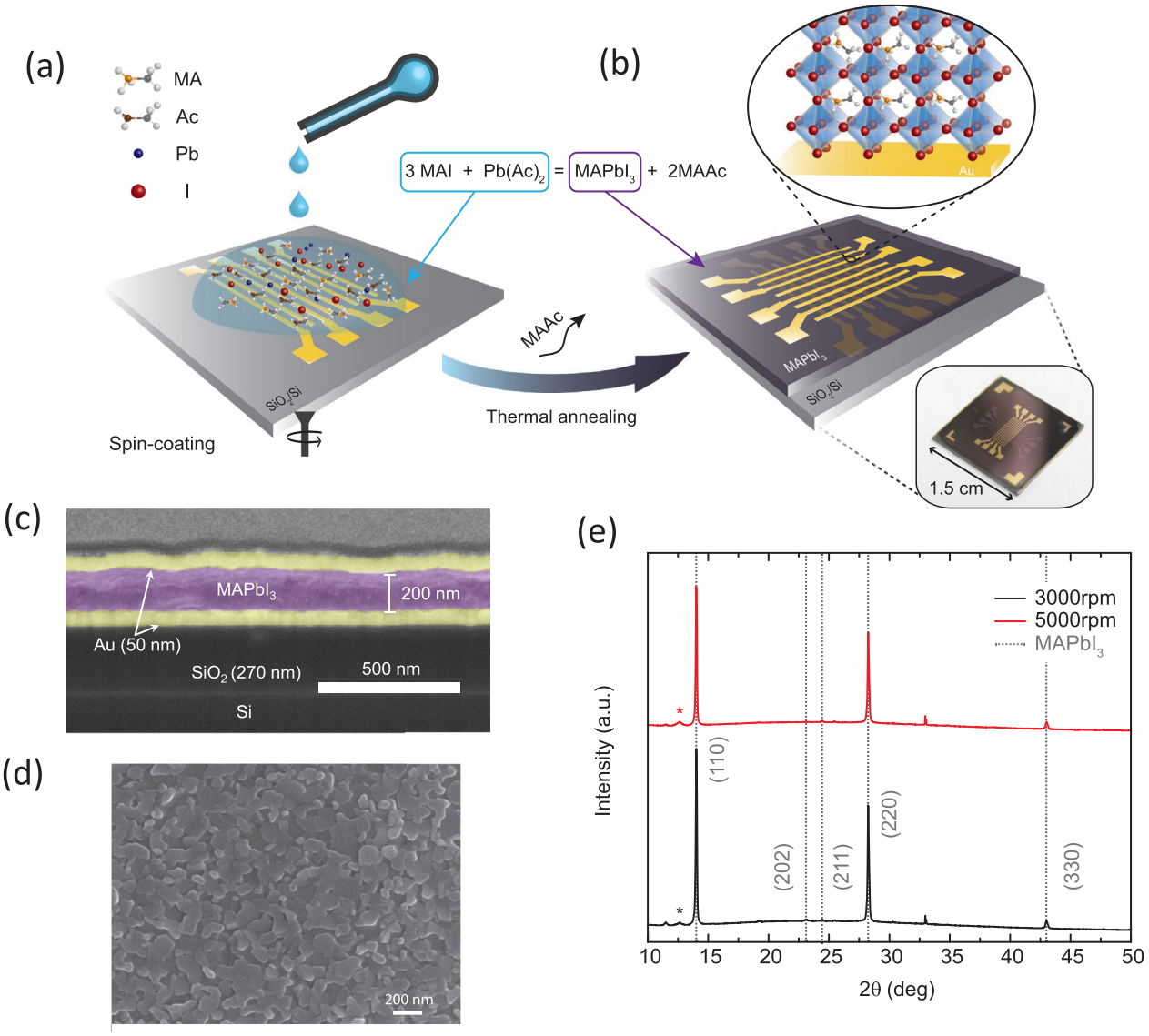

Figure 1. a) A schematic image of the fabrication process for $MAPbI_3$ perovskite memory devices. The precursors used in the solution, MAI, and $PbAc_2$ are represented as molecules (defined in the legend). Note that the solvent molecules and the charge on each molecule are neglected for simplicity. b) A schematic image of the final $Au/MAPbI_3/Au$ memory devices in 8×8 cross-bar array architecture. The top inset represents the crystal structure of $MAPbI_3$ formed on top of the bottom Au electrode, and the bottom inset shows a photograph of the fabricated devices. c) A cross-sectional SEM image of the $Au/MAPbI_3/Au$ on a SiO_2/Si substrate. d) The top-surface FE-SEM image of a $MAPbI_3$ film. e) XRD spectra of $MAPbI_3$ films spin-coated at 3000 rpm (red line) and 5000 rpm (black line) with peaks (positions indicated from gray dashed lines) assigned to the reflections from a tetragonal $MAPbI_3$ perovskite lattice unit cell.[25] The peak marked as * is a trace of a small amount of PbI_2.

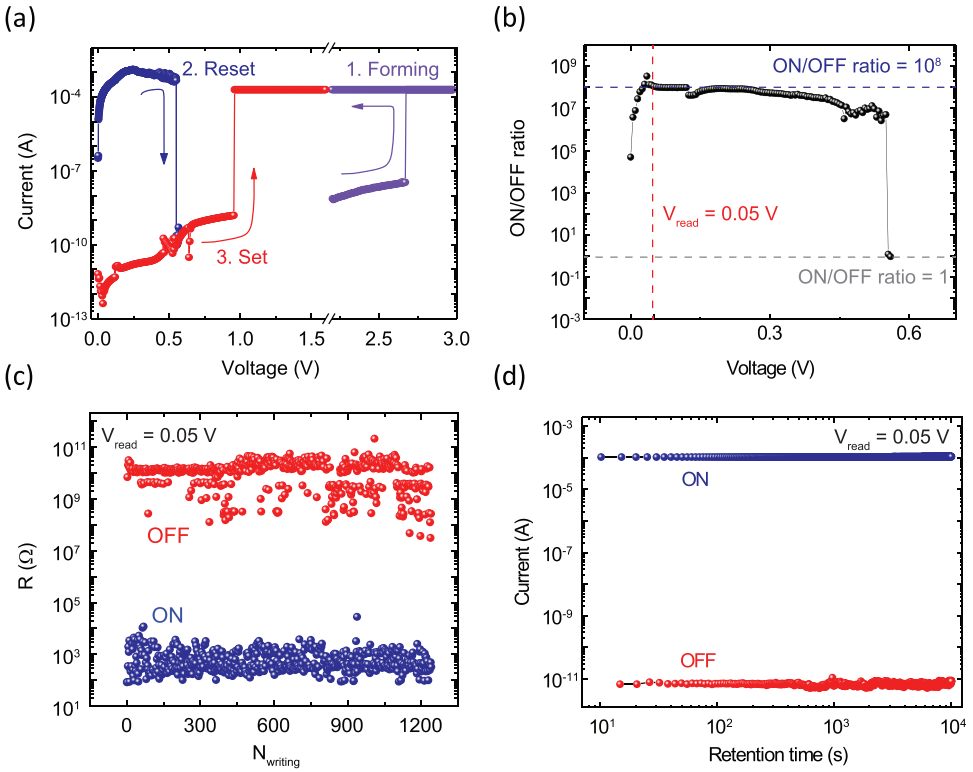

Figure 2. a) A representative *I–V* graph of a unipolar Au/$MAPbI_3$/Au device. b) The ON/OFF ratio is plotted as a function of voltage. c) The electrical endurance test and d) the retention test results for the $MAPbI_3$ perovskite memory device. The blue and red colors represent the current values of the LRS (ON) and HRS (OFF) states, respectively.

$PbCl_2$ and PbI_2) is caused by an accelerated perovskite growth kinetics in the case of the $PbAc_2$-based film in which the side-product, MAAc, is highly volatile and is therefore quickly driven out of the film during the early stage of the deposition.[25]

The structure of the resulting perovskite film is shown by cross-sectional and top-surface images measured by a field emission scanning electron microscope (FE-SEM) (Figure 1c,d, respectively). We can identify that Au electrodes are clearly separated by a compact $MAPbI_3$ film in a cross-sectional image of a Au/$MAPbI_3$/Au device (Figure 1c). From the top-view FE-SEM image (Figure 1d), a typical size of the grains formed in the film was found to be ≈150 nm, which is a similar value compared to that reported in the literature.[26] More FE-SEM images are available in Figure S1 (Supporting Information). The crystal structure of the $MAPbI_3$ film was confirmed to be identical to that of a film deposited via a conventional PbI_2 precursor[25] according to X-ray diffraction (XRD) data (Figure 1e), except that the peak corresponding to PbI_2 at $2\theta = 12.5°$ is significantly smaller in the $PbAc_2$-based film. This result reflects a more complete conversion of the precursors to perovskite crystals in our film compared to the conventional spin-coating method.[26] The reflection at $2\theta = 33°$ could be due to the reflection from the SiO_2/Si substrate as shown in Figure S2 (Supporting Information). In addition to the compactness of the film deposited from $PbAc_2$, the film was found to be smooth, with a rms roughness of ≈9 nm, as confirmed by atomic force microscope measurements (see Figure S3 in the Supporting Information); this roughness is significantly lower than that in the PbI_2-based films deposited from a solvent-dropping method (typically, rms roughness is in the range of 50–110 nm).[24,25] The high-quality perovskite film is an essential requirement in achieving high-yield memory devices (see Section S1D in the Supporting Information).

To investigate the properties of our memory cells, we first fabricated 1 × 8 cross-bar array memory cells with the perovskite film deposited as described above. The memory cells showed typical current–voltage (*I–V*) characteristics that represent unipolar resistive switching behaviors, as shown in **Figure 2**a. The first *I–V* sweep of the memory cell (indicated as process 1 in Figure 2a), originally in the high-resistance state (HRS or OFF state), underwent forming at a typically high voltage (of ≈2.7 V), while the compliance current was set to 200 µA. The device switched to low-resistance state (LRS or ON state) during the forming process. The reset process (process 2 in Figure 2a) involved a subsequent *I–V* sweep from 0 V under no compliance. The current increased beyond the compliance current set in the forming process and underwent a rapid reduction in the current at 0.55 V which is the reset voltage. The memory cell was then switched back to HRS. The HRS could be switched to LRS again via the set process which was a new *I–V* sweep starting from 0 V (process 3 in Figure 2a). The current increased rapidly at ≈0.96 V, which is the set voltage. Note that these characteristics unambiguously represent unipolar resistive switching and resemble that of well-established unipolar metal-oxide-based resistive memory devices made with TiO_2, SiO_x, and NiO_x.[27–31] To the best of our knowledge, our work is the first detailed study of unipolar resistive switching in organic metal halide perovskite, in contrast to

bipolar resistive switching, which has typically been observed in perovskite memory devices in previous studies.[13–17]

The relatively low-voltage operation demonstrated above is a common feature of perovskite resistive memory devices.[13–17] The average set and reset voltages in our study were 1.16 and 0.46 V, respectively, with a certain distribution (see Figure S9 in the Supporting Information). Based on the thickness (200 nm) of the perovskite film determined by the cross-sectional scanning electron microscope (SEM) image (Figure 1c), the average electric field required for set and reset were 5.8 and 2.3 MV m^{-1}, respectively, the same order of magnitude as those of the reported bipolar memory devices based on organo-metal iodide perovskite.[14–16] From the *I–V* curves in Figure 2a, we determined the ON/OFF ratio in our perovskite memory devices to be $\approx 10^8$ (Figure 2b), which can be considered a high ON/OFF ratio reported for the resistive memories fabricated with various types of materials. We have compared the memory performance of our devices with other types of various memory devices, as summarized in Section S3 (Supporting Information).

In addition to the excellent ON/OFF ratio and the low-voltage operation of the perovskite resistive memory devices, the memory showed stable electrical characteristics from both a relatively large endurance of >1000 writings with the average ON/OFF ratio $\approx 2 \times 10^7$ (see Section S5 in the Supporting Information for more details) and a long retention time of over 10^4 s (Figure 2c,d). The reading voltage was chosen as 0.05 V in order to avoid unintentional switching of the memory devices during the measurements. The memory devices also exhibited stable multilevel resistance states that could be accessed by using different compliance currents during the set process (see Figure S13 in the Supporting Information). In addition, the air stability of our unipolar perovskite memory was confirmed from a relatively stable operation with a large ON/OFF ratio between 10^5 and 10^6 up to 30 days of storage in an ambient condition. Moreover, we observed a fast switching of 81 µs for the set process and 2 µs for the reset process by tracing the current responses during the pulse measurements (see Figure S17 in the Supporting Information); these fast switching performances are critical for high-frequency operation for practical memory devices. Although pulse operations with a short pulse width (down to 200 ns[32]) has been reported for perovskite memories,[14,16,17,24,32,33] there have been only a few reports that directly showed the current response during a short-pulse operation.[17]

Our perovskite memory devices are unique in that they exhibit unipolar (or nonpolar) resistive switching unlike most of the reported $MAPbI_3$ and other solution-processed perovskite-based memory devices, which showed bipolar resistive switching (see Table S1 in the Supporting Information). The main difference of our memory device is that we employed symmetric Au electrodes (Au/$MAPbI_3$/Au) unlike the other studies. Since Au is unlikely to react electrochemically, any resistive switching mechanisms that involve redox reaction between active metal ions (e.g., Ag) and a counter electrode[16,24] or halide ions[17] are inappropriate.

One of the widely accepted mechanisms for explaining the nonpolarity of unipolar resistive memory devices is the formation and rupture of conducting paths composed of anion vacancies via a dominant role of a thermal driving force generated by Joule heating rather than the role of the electric field.[30] In light of the resistive switching mechanism for oxide-based unipolar memory devices, many of which show *I–V* characteristics that resemble our unipolar perovskite memory devices (e.g., NiO,[34] TiO_2,[35] Ga_2O_3,[36] Fe_2O_3,[37] and ZnO[38]), a similar mechanism can be proposed by considering iodine ion vacancies (V_I's) instead of oxygen vacancies. The formation and dissolution of the conducting paths can be explained in terms of two competing forces that drive the diffusion of halide ion vacancies; one via a thermal gradient (Soret force) and one via a vacancy concentration gradient (Fick force) both of which are induced by Joule heating[28,31] (see Section S9 in the Supporting Information for more details).

A closer examination of a typical *I–V* curve of our perovskite memory devices (see Figure S20a in the Supporting Information) reveals some information regarding underlying physical processes during unipolar resistive switching events in perovskite memory devices. The *I–V* curve for the HRS during the set process can be fitted linearly in a low-voltage regime (<0.1 V), and the shape of the curve becomes quadratic for voltages above 0.4 V. This may reflect a transition from an Ohmic conduction of intrinsic charge carriers in the perovskite film at the lower-voltage range to a space-charge limited current regime at the higher-voltage range.[39,40] The temperature dependence of the HRS current shows a thermally activated transport with a relatively large activation energy of 0.31 eV (see Section S9 in the Supporting Information for more details), which is presumably due to a larger grain boundary density for our $PbAc_2$-driven $MAPbI_3$ films. This leads to a larger effective energy barrier for charge transport in HRS (a larger HRS resistance) and thus enables one of the best ON/OFF ratios (maximum above 10^8) reported for solution-processed memory devices (see Table S1, Supporting Information).

A large increase in the current at the set voltage (≈0.96 V) (Figure 2a) reflects the formation of highly conducting paths. The nature of the conducting paths is yet to be confirmed; however, they are likely to be composed of ion vacancies, especially iodide ion vacancies (V_I's) because the theoretically predicted activation energy for halide ion migration is lower than that of MA and Pb ions.[41–46] Zhu et al. also observed that an aggregation of V_I's occurred in the $MAPbI_3$ film upon an applied lateral electric field via iodide ion migration.[17] According to first principles calculations, the V_I's can act as donors[47,48] and thus the V_I-rich regions can act as highly conducting paths, which can result in switching to the LRS. Indeed, the *I–V* curve of the ON state at a low voltage during the reset process shows an Ohmic conduction characteristic (see Figure S20b in the Supporting Information), which indicates that the conducting paths are metallic filaments. The metallic conduction of LRS is also confirmed from a linear temperature dependence of the LRS resistance (see Figure S21b in the Supporting Information). During the reset process, the conduction became slightly nonlinear at a higher voltage (above 0.3 V) (see Figure S20b in the Supporting Information), which is indicative of localized Joule heating (i.e., higher resistance of the metallic filaments via the locally raised temperature) before the device underwent reset at 0.4 V. This is in agreement with the significant role of the Joule heating in the dissolution of the conducting paths of our proposed

mechanism for unipolar resistive switching (see Section S9 in the Supporting Information for more details).

Despite a continuous search for solution-processed perovskite material variants that exhibit resistive switching,[23,24,49–52] most of the device architectures for perovskite RRAM have been limited to dot-array structures. There have only been a few reports that directly demonstrated the integration of the perovskite RRAM devices in a cross-bar architecture. For example, Hwang et al. recently employed a sequential vapor-deposition method to produce a uniform perovskite film in cross-bar array perovskite memory devices.[32] In our study, we fabricated high-yield perovskite memory devices in an 8 × 8 cross-bar array structure with the solution-processed perovskite film deposited with $PbAc_2$. The resistances values of the LRS and HRS of each memory cell (64 cells in total) are shown as color maps in **Figure 3**a and Figure 3b, respectively. The yield of the memory devices was found to be ≈86% (55 devices out of 64 devices were functional) (Figure 3a,b). The nine devices that could not be turned off (see Figure 3a) were short-circuited after the forming process. In addition, the device-to-device variation was found to be small. The resistance values of the LRS and HRS are plotted cell by cell in Figure 3c. The plot reflects well-defined bistable states in our perovskite memory devices in the cross-bar array structure. In particular, the high average ON/OFF ratio of 10^6 is unprecedented in cross-bar array perovskite RRAM devices. Moreover, the distributions of the resistance values of LRS and HRS were found to be narrow; ≈1 order of magnitude range for LRS and ≈2 orders of magnitude range for HRS (see the insets of Figure 3a,b,d). The maximum LRS resistance was found to be ≈2×10^4 times smaller than the minimum HRS resistance. The distribution of the set and reset voltages of the working memory cells can be found in Figure S22 (Supporting Information). A good in-wafer uniformity of the crossbar-array device is also supported from the data for a crossbar-array device with the device yield of 94% (presented in Section S11 in the Supporting Information). The in-wafer uniformity of set and reset operation voltages is a critical requirement for an accurate operation of large crossbar-array memory devices. Although the overlap between the set and reset voltage distributions was found to be finite for the cross-bar array devices, our calculation results show that its effect is not significantly large to induce erase failure (see Section S12 in the Supporting Information for more details). On the other hand, the wafer-to-wafer uniformity was found to be slightly worse than the in-wafer uniformity perhaps due to a small batch-to-batch morphology variation of the perovskite films (see Section S13 in the Supporting Information for more details).

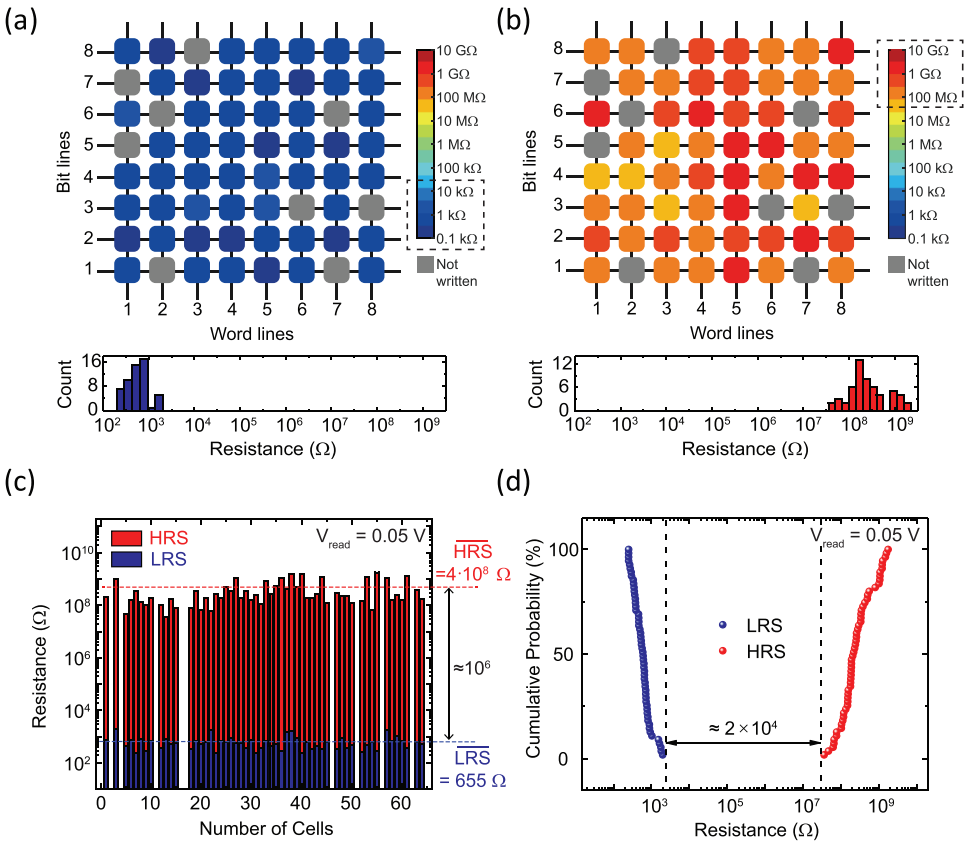

Figure 3. a,b) The color map plots of the resistance distribution of the 64 memory cells in the LRS (a) and HRS (b). The cells shown as gray were found to be short-circuited. The color scale bar shown on the right of each plot represents the corresponding resistance values. The plots shown at the bottom represent the histograms of the resistance values for the memory cells in the LRS (a) and HRS (b). c) The resistance values of the LRS (blue) and HRS (red) plotted for memory cells. The blank regions represent the short-circuited cells. The average resistance values of the LRS and HRS are indicated on the right. d) The cumulative probability plot for the resistance values of the LRS and HRS.

Although the crossbar-array structure guarantees an excellent scaling potential, the pure passive cross-bar array structure suffers from cross-talk interference between interconnected memory cells, thereby preventing a reliable reading operation of a selected memory cell due to parasitic conducting paths composed of interconnects and the neighboring cells.[53,54] Here, we demonstrate that the cross-talk interference can be significantly reduced by employing the 1D–1R scheme[3,55–57] in perovskite RRAM devices connected to external diodes. The 1D–1R scheme is feasible with memory cells that exhibit unipolar resistive switching[58] (i.e., the set and reset voltages have the same polarity), in contrast to most of the reported perovskite RRAM devices which showed bipolar resistive switching.[14–16] Before integrating external diode elements for achieving the 1D–1R scheme, we note that the requirements for the diodes are quite strict because of the low operation voltages of the perovskite memory cells. Therefore, we employed commercial diodes (1N4007 Fairchild Semiconductor) with a low operation voltage to examine their compatibilities with the perovskite memory devices exhibiting typical *I–V* characteristics shown in **Figure 4**a. The diode shows a good rectification ratio of $\approx 1.5 \times 10^5$ at the voltage of 0.5 V (chosen as the reading voltage). When electrically connected in a series with the unipolar perovskite memory cells (typical *I–V* characteristics shown in Figure 4b), the resulting 1D–1R cell showed a current-rectified property (Figure 4c). The set voltage remained the same when the memory cell was connected to the diode, whereas the reset voltage shifted to a higher voltage due to an extra series resistance from the diode (see Figure S31 in the Supporting Information). The diode has a finite on-current limit at the voltage below 0.5 V and limits the current through the whole circuit. This may result in an insufficient amount of Joule heating required for the reset process, as explained above. In addition, the ON/OFF ratio is still high ($\approx 10^5$) but lower than the average ON/OFF ratio of the memory cells alone due to the finite resistance of the diode. The 1D–1R cell also preserved a reliable retention (longer than 10^4 s) and stable electrical endurance properties (more than 500 writings with the average ON/OFF ratio $\approx 2 \times 10^4$) of the original $MAPbI_3$ perovskite memory cell (see Figures S28 and S29 in the Supporting Information). In addition, the 1D–1R cell exhibited a favorable electrical stability from a significantly smaller variation of the ON/OFF ratio (and the distributions of LRS and HRS resistance values) during the endurance than that of the 1R cell, as well as smaller overlap between the set and reset voltage distributions, which are essential for a reliable memory operation (see Section S14 in the Supporting Information for more details).

In a pure passive cross-bar array structure of memory cells (1R array), neighboring 2 × 2 cells can be described with an equivalent circuit of one memory cell and three memory cells in parallel connection. The total current measured in this circuit, I_{total}, will be a combination of the current through a selected cell, $I_{OFF,}$ and the parasitic current through the three cells, I_{sneak}. This is known as the cross-talk phenomenon, which induces misreading of a selected memory cell. When we read the resistance of an OFF cell ((1,1) in Figure 4d) surrounded by three neighboring cells ((1,2), (2,2), and (2,1) in Figure 4d) that were turned ON, the measured resistance of 508 Ω (see Figure 4e) nearly corresponded to that of an ON state. Therefore, this leakage current through the sneak path, I_{sneak} (shown in Figure 4d), prevents a selective reading/operation of memory cells because it is much larger than I_{OFF}. This also ultimately limits the overall scaling advantage of RRAM because of the requirements for relatively large sensing circuits to prevent reading errors.[53] In this study, we demonstrate an effective 1D–1R scheme by connecting four different memory cells through an external circuit that contains four diodes via wire bonding (see Figure 4f and Figure S32, Supporting Information). Different from the four neighboring cells in 1R array (above), the resistance value read for the (1,1) cell clearly showed the reduction in the cross-talk. The read resistance was found to be 270 MΩ at the read voltage of 0.5 V, even if the (1,2), (2,1), and (2,2) cells were all turned ON (i.e., their resistance values were more than four orders of magnitude lower than that of the (1,1) cell) (see Figure 4g). This is a clear indication that the I_{sneak} is suppressed by the diodes that are connected in opposite configurations to one another in the parasitic current path that connects the cells (1,2), (2,1), and (2,2) (see Figure 4g for the equivalent circuit representation). Our results demonstrated the selective operation of unipolar perovskite memory cells in 1D–1R scheme. Note that the resistance measurement was performed after carefully checking the resistance and electrical connection of each component in the connected circuit in order to eliminate any artifacts in the measurement (see Figures S33 and S34 in the Supporting Information). We have also calculated the read voltage margin of $N \times N$ crossbar-array device made of our 1D–1R perovskite memory cell in order to estimate the maximum memory size achievable when one bit line pull-up read scheme is employed (see Section S16 in the Supporting Information).[53,59] The read margin remained above 10% up to $N = 830$, yielding the maximum memory size of 689 kbit, which is significantly larger than the estimated maximum memory size for other previously reported 1D–1R memory based on organic materials[55–57] and many of the inorganic materials (see Table S3 in the Supporting Information for more details).[60–62] In overall, our demonstration of suppressed cross-talk interference and the read voltage margin analysis can be taken further and used as guidelines for developing a large array size on-chip 1D–1R perovskite memory architecture.

Our results demonstrate high-performance resistive memory devices based on organo-metal halide ($MAPbI_3$) perovskite films prepared with a $PbAc_2$ precursor via a simple single-step spin-coating method. The perovskite memory devices exhibited a unipolar resistive switching behavior in Au/$MAPbI_3$/Au structure with a high ON/OFF ratio of up to 10^8 and with an excellent stability, as confirmed from the endurance (more than 1000 writing cycles) and retention (>10^4 s) test results. In addition, the reliability of the perovskite memory devices integrated in an 8 × 8 cross-bar array architecture was demonstrated, achieving a high yield of up to 94% and uniform memory cell characteristics. Furthermore, the demonstration of 1D–1R scheme using our perovskite memory devices demonstrated a selective operation of memory cells by suppressing the cross-talk interference between neighboring cells connected via external diodes. These results are highly relevant for realizing low-cost and high-density practical perovskite memory devices via a simple solution process.

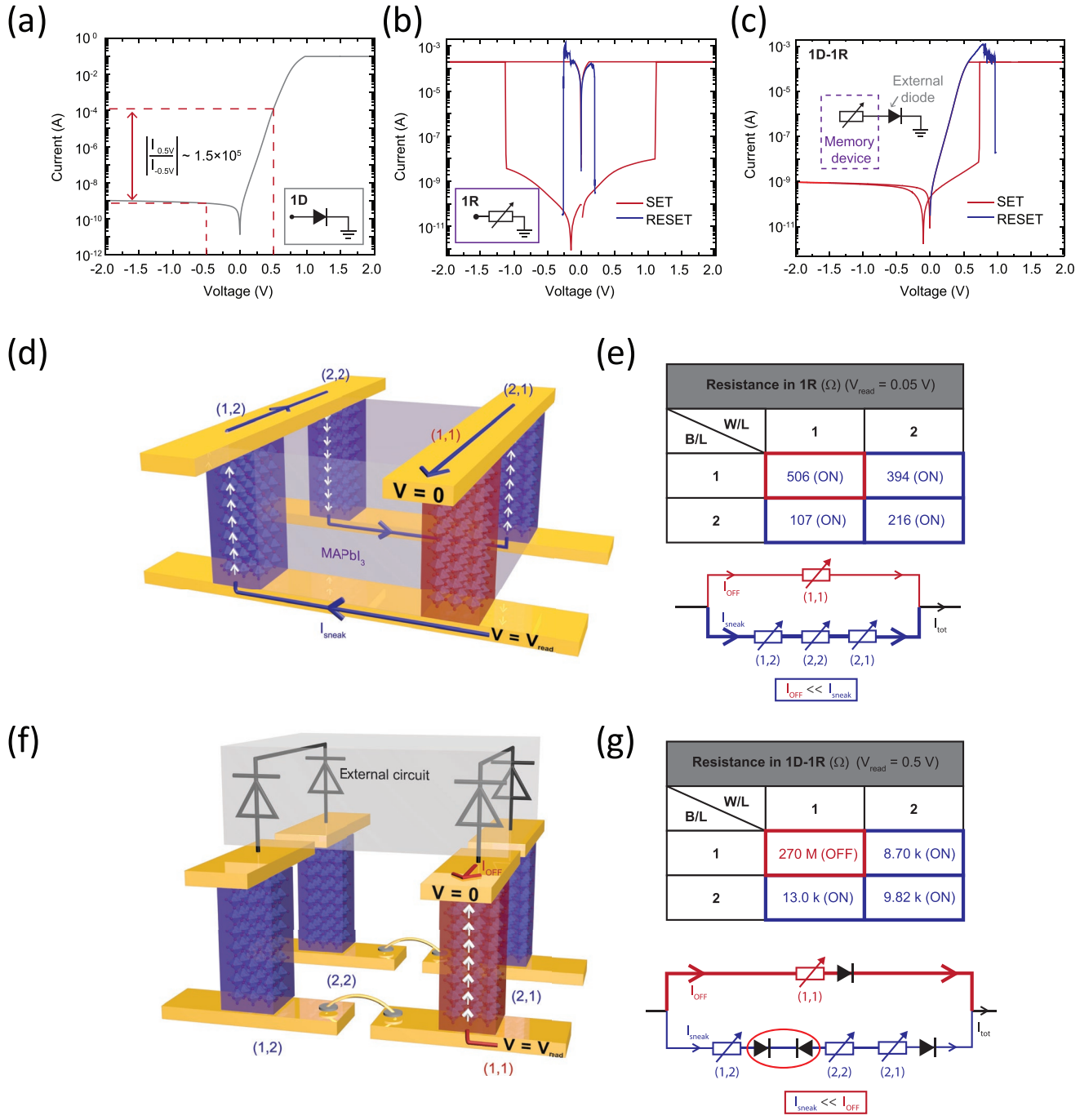

Figure 4. a) The *I–V* curve of the external diode used for the 1D–1R scheme. b) A typical *I–V* curve of the unipolar perovskite memory device used for the 1D–1R scheme. c) The *I–V* curve of the diode and the memory device connected in series, showing a rectification behavior. d) A schematic diagram illustrating the reading operation of the (1,1) cell in a 2 × 2 array memory cells. Cross-talk interference due to a sneak-path current, I_{sneak} (the path shown in blue), is observed when V_{read} of 0.5 V is applied between the first bit line (B/L) and the first write line (W/L). e) The resistance values of each cell (top) and the equivalent circuit of the 2 × 2 array memory cells (bottom). f) A schematic illustration of the same reading operation in a 2 × 2 array in 1D–1R scheme with memory cells connected by external diodes. g) The resistance values of each cell (top) and the equivalent circuit of the 2 × 2 array memory cells in 1D–1R scheme. I_{sneak} is suppressed by the diodes connected in the opposite polarities (circled in red as an example).

Experimental Section

Device Fabrication: Au bottom electrodes with linewidths of 50 µm and a thickness of 50 nm were deposited by e-beam evaporation through a shadow mask on cleaned SiO_2/Si substrates. Two different shadow masks were used when depositing the bottom Au electrodes for 1 × 8 and 8 × 8 cross-bar array devices. The bottom electrodes and the substrate were treated with UV–ozone illumination for cleaning. The $MAPbI_3$ solution was made from solution mixtures of MAI and $PbAc_2$ dissolved in *N*,*N*-dimethylformamide at a 3:1 molar ratio to make the

concentration of 0.75 M. MAI was ordered from Dyesol (CAS#: 14 965-49-2) and $PbAc_2$ was ordered from Sigma-Aldrich (CAS#: 6080-56-4). The solution was stirred for 30 min while being heated on a hotplate at 60 °C. The heated solution was spin-coated onto the bottom electrodes in a controlled environment inside a glovebox at a rate of 3000 or 5000 rpm for 45 s. After leaving the sample for 10 min at room temperature to allow evaporation of remaining solvent in the sample, the sample was heated at 100 °C for 5 min to initiate the formation of $MAPbI_3$ crystals. The top Au electrodes with linewidths of 50 μm and a thickness of 100 nm were deposited through a shadow mask by electron beam evaporation. The memory cell size was defined as 50 μm × 50 μm.

Device Characterization: The electrical measurements were performed using a semiconductor parameter analyzer (Keithley 4200 SCS) in a vacuum environment (≈10^{-3} Torr). The scan rate of the voltage sweep in *I–V* measurements was typically 0.54 V s^{-1}. The voltage bias was applied to the top Au electrode while the bottom Au bottom was grounded.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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