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Miniaturization and Integration of Organic Resistive Memory Devices

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Recently, organic resistive memory devices have attracted great interest because they can be fabricated to low cost, flexible, and printable memory cells. Here, we reviewed recent advances of miniaturization and integration of organic resistive memory devices. We introduced research background of fabrication of organic resistive memory devices. Then we arranged achievements on miniaturization and integration of organic resistive memory devices in chronological order. Finally, we summarized research outlook of miniaturization and integration of organic resistive memory devices.

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I. INTRODUCTION

Because conventional silicon-based technologies are common in the storage media, the demands for better integration densities and advanced device performance are continuously extending. Silicon-based technologies are currently facing the theoretical and physical limits of downscaling [1–5]. This hindrance to information storage has triggered the development of novel memory technologies that are principally based on the bistability of materials that arises from changes in intrinsic properties such as ferroelectricity, magnetism polarity, phase, conformation and conductivity. These emerging technologies include ferroelectric memory, magnetoresistive memory, phase-change memory, and resistive memory [1–5]. In particular, the organic-based resistive memory developed have been considered to be a promising candidate for next-generation nonvolatile memory devices [6–11]. With this regard, resistive memory devices have been attracted great interest from both industrial and academic researchers in the last decade. Resistive memory devices, which have two-terminal structure, change their resistance by modulating the applied bias [12]. In succession to the success of oxide-based inorganic resistive memory devices regarding fast data storage speed, high data storage integration capability (cross-bar architecture), and stable storage endurance, resistive memory devices are possibly considered to be a next generation to flash memory devices. Along the development of the oxide-based resistive memory devices, organic memory device has been considered to be promising candidate as next-information storage devices due to its advantages such as low cost, ease of fabrication, large-area processibility, material variety, flexibility and printability of organic-based materials [12–15]. Organic resistive memory devices have often been fabricated in a simple dot array or cross-bar structure, which can realize high integration of memory cells.

While silicon based industry has achieved integration of nano-sized electronic devices, organic memory devices have usually been limited to be less than a hundred bits integration with the individual cell size of several hundreds of microns, which usually were fabricated by shadow mask method for top electrode formation. The conventional photolithographic patterning technique to scale down the devices has been considered to be inadequate to organic electronics because of the chemical incompatibility between organic electronic materials and organic solvents for photolithographic processing. Because of this issue, some researchers focused on designing alternative technique to miniaturize and integrate the organic resistive memory devices. In this review article, several methods for miniaturization and integration of the organic resistive memory devices are introduced, which are conventional photolithography method on photo cross-linked copolymer, *via* hole structure method, direct metal transfer method, conventional photolithography with buffer layer, orthogonal photolithography method with fluorinated photoresist and miniaturization *via* nanostructure grown. Various miniaturization methods listed above are introduced in Table 1.

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Table 1. Various miniaturization and integration techniques for organic resistive memory devices.

Method	Material	Electrodes (T,B)	Mmory type	Array type	Cell size (μm^2)	Actual Integration	Delnsity of cells (cells/mm^2)	Device Yield
Common photolitho on photo cross-linkable copolymer (2007)	PFN-C	Al,Au	Write once (WORM)	Crossbar	4	2×2	62500	-
Via-hole structure (2009)	WPF-oxy-F	Ag,p+ Si	Bipolar	Dot array	0.04	-	6250000	-
Direct metal transfer (2008,2011)	WPF-oxy-F	Ag,p+ Si	Bipolar	Crossbar	4	8×8	62500	64%
	PI:PCBM	Au,Al	Unipolar	Crossbar	0.01 - 4	8×8	62500 - 25000000	78% for microscale devices
Conventional photolithography using buffer layer (2012)	PI:PCBM	Au,Al	Unipolar	Crossbar	16	8×8	15625	-
Orthogonal photolithography (2015)	PI:PCBM	Au,Al	Unipolar	Crossbar	50 - 100	64×64	2500	79.6%
Glancing angle deposition (2017)	α-NPD	Au (STM tip), Ag/ITO	Bipolar	Nanocolumn	~ 0.01	-	25000000	-

II. MINIATURATION AND INTEGRATION OF ORGANIC RESISTIVE MEMORY

1. Conventional photolithography on photo cross-linked copolymer

A multi-stackable memory device was fabricated using a photo cross-linkable copolymer by Kwan *et al.* [16]. When it was cross-linked, the polymer film became immiscible, making multi-level stacking possible. Kwan *et al.* has pointed that the polymer for organic resistive memory must be robust enough to withstand lithographic processes that are used in the patterning of the electrodes. It must also not be dissolved by its own solvent again when the bottom layer polymer film is deposited. However, most polymer blend or copolymer systems reported so far are miscible in common solvent, thus common photolithography method cannot be applied on them. Kwan *et al.* employed photo cross-linkable copolymer (PFN-C), which was synthesized using Suzuki polycondensation. The spin-cast film of the polymer solution (3.0 wt% PFN-C, 0.4 wt% PAG 203 (photoacid generator in 1,2dichlorobenzene) was irradiated with UV light through a photo mask. The substrate was then placed on a 90 °C hot plate for 2 min and rinsed in toluene. It was finally baked on the hot plate at 150 °C for 30 min to complete the cross-linking process. Thermogravimetric analysis of PFN-C showed that it remained stable up to 200 °C after cross-linking. To fabricate a resistive memory device, a silicon wafer with thermally grown oxide was used as the substrate. The bottom Au electrode was first patterened using the common photolithography. The polymer solution was then spin-coated on the substrate and cured using UV light. The thickness of the film was about 65 nm. As PFN-C became insoluble after the cross-linking process, the lift-off method could be used to pattern the top Al electrode deposited on the polymer film (Fig. 1(c)). The microscale memory device with 4 μm × 4 μm exhibited normal switching current-voltage (I-V) characteristics (Fig. 1(d)). Then, a vertically stacked array was fabricated. The bottom aluminum electrode was first deposited on a glass substrate using shadow mask. The bottom polymer film was then spin-coated. The same processes were then repeated for the middle electrodes, the top polymer film and the top electrodes. Figure 1(e) shows that both bottom and top devices showed similar electrical characteristics as the single layer device. Kwan *et al.* secured the robustness of the organic material by using cross-linking process [16]. However, this method can only be applied to the specific polymer material which have cross-linkable functional group, meaning incompatibility with general organic circuit or chip.

2. *Via* hole structure

With above scaling issues of using cross-linkable polymer, in 2009, Kim *et al.* suggested a *via*-hole structure as a scalable test-bed for switching characterization of polymer materials [17]. Kim *et al.* focused on understanding of the memory operation mechanism by memory miniaturization to sub-micron scale although *via*-hole structure could not be a practical application for the organic resistive memory, In this regard, miniaturized polymer memory devices in a *via*-hole structure were fabricated on a heavily doped p-type (100) silicon (p+ Si) substrate (Fig. 2). After the typical ultrasonic cleaning process with acetone, methanol, and deionized (DI) water, the silicon substrate was treated *via* a diluted HF-last process to remove the native oxide layer. To make *via*-hole structures, $\sim$ 100 nm thick silicon oxide film was deposited on the silicon substrate using plasma-enhanced chemical vapor deposition (PECVD). The hole to be filled with the polymer memory devices was defined by electron beam lithography in the *via*-hole structures, which had five different square cells with side length: 40 μm, 8.5 μm, 4.5 μm, 1 μm, 500 nm,

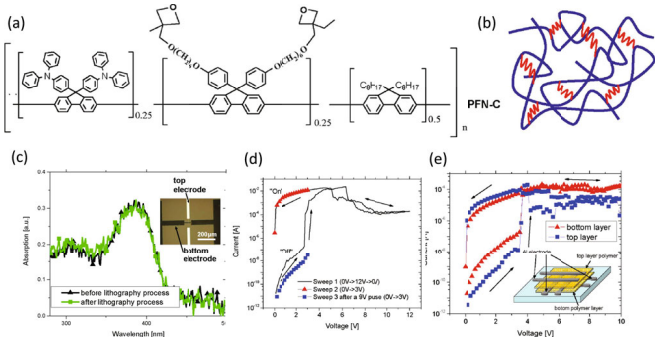

Fig. 1. (Color online) Common photolithography on photo cross-linkable copolymer. (a) Chemical structure of photo cross-linkable polymer, PFN-C. (b) After cross-linking, a network of polymer chain is formed, increasing robustness. (c) Absorption spectra of PFN-C before and after the lithography process did not change, indicating that PFN-C was not removed during the process. Inset: Microscope image of a 4 μm × 4 μm memory device. (d) Current-voltage characteristics. (e) Current-voltage characteristics of the double-stacking memory device.

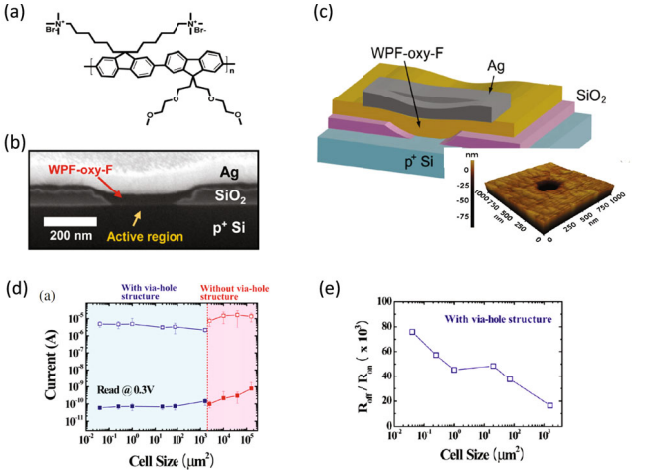

Fig. 2. (Color online) *Via*-hole structure. (a) Chemical structure of WPF-oxy-F polyfluorene derivative. (b) Schematic of a polymer memory device in a *via*-hole structure. (c) AFM image of a *via*-hole of area 200 nm × 200 nm. (d) Current values of ON and OFF states of polymer memory devices as a function of active area. (e) Dependence of the OFF/ON resistance ratio of polymer memory devices as a function of active area.

and 200 nm. To expose the bottom electrode through a *via*-hole, the silicon oxide film was etched out using 6 : 1 buffered oxide etchant (BOE). Finally, to fill the *via*-hole with the polymer memory materials using a spin-coating method, they used the isotropic property of a wet etching process. As a result of wet etching, the slope of the *via*-hole well became gently inclined, so that the polymer materials could easily be spin-coated and filled in the *via*-hole reducing pores or defects. Poly[(9,9-bis((6'-(N,N,N-trimethylammonium)hexyl)-2, 7-fluorene)-alt-(9,9-bis(2-(2-methoxyethoxy)ethyl)-fluorene))] dibromide (WPF-oxy-F) was used as active polymer memory layer [18]. WPF-oxy-F dissolved in methanol at a concentration of 5 mg ml-1 was spin coated on the substrate at 2000 rpm for 30 s. Post baking was performed at 150 °C for 20 min on a hot plate in a nitrogen-filled glove box. The thickness of the memory film in the *via*-hole was about 70 nm. To make the top electrodes on the polymer layer in the *via*-hole structure, a shadow mask was aligned and a 100 nm thick Ag layer was deposited using a thermal evaporator under a pressure of 10^{-6} Torr. In Fig. 2, the details of device structure are shown. Usually, WPF-oxy-F resistive memory fabricated by shadow mask (hundreds microns size) exhibits bipolar switching property, where set voltage and reset voltage have opposite bias direction. The *via*-hole structure WPF-oxy-F memory also exhibited typical bipolar switching characteristics in 500 nm × 500 nm cell size. In Figs. 2(d) and 2(e), the current value of the ON state did not change with variation of the active area (about 5 μA), whereas the current value of the OFF state decreased slightly as the active area decreased. Since the formation of localized current at the first spot (filament) may prevent the activation of current flows through other spots, the ON state current shows area independent behavior. On the other hand, because the OFF state current flow is limited by the leakage current, it is proportional to the active area of the device. Therefore, the ON/OFF ratio (R_{OFF}/R_{ON}) also increased slightly as the active area decreased. These observations indicated that localized current paths (conducting filaments) are formed and affect the resistive switching behavior even in sub-micron scale *via*-hole polymer memory devices. If the resistive switching behavior is governed only by filamentary conduction, the OFF state current should scale with the active area. These dependences on the active area implied that SCLC with filamentary conduction is the origin of the resistive switching behavior. The *via*-hole method exhibited excellent possibility that organic resistive memory can be scaled down to several hundred micron [17]. However, because of the hole-structure, cross-point architecture cannot be fabricated by this method, which fundamentally obstructs the genuine integration of organic resistive memory devices.

3. Direct metal transfer method

It is necessary to introduce an alternative fabrication process that can obtain high memory density and use non-aqueous fabrication methods which do not damage organic memory layer. Stamp methods which directly transfer metal electrodes on a flat sample can be one promising candidate. Cold-welding, micro contact printing or nanoscale transfer printing have demonstrated highly integration of organic or molecular devices [19–

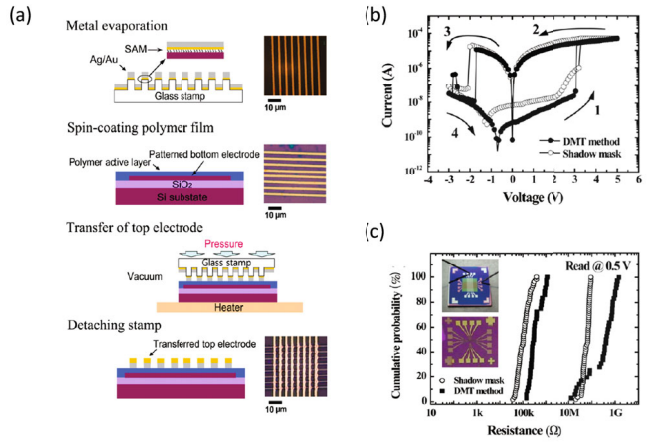

Fig. 3. (Color online) Direct metal transfer (2008). (a) Fabrication process of cross-bar type polymer non-volatile memory devices using DMT method. (b) Switching characteristics of memory cells in cross-bar arrays fabricated by the DMT and shadow mask methods. (c) Cumulative probability data for 8×8 cell array memory devices fabricated by the DMT and shadow mask.

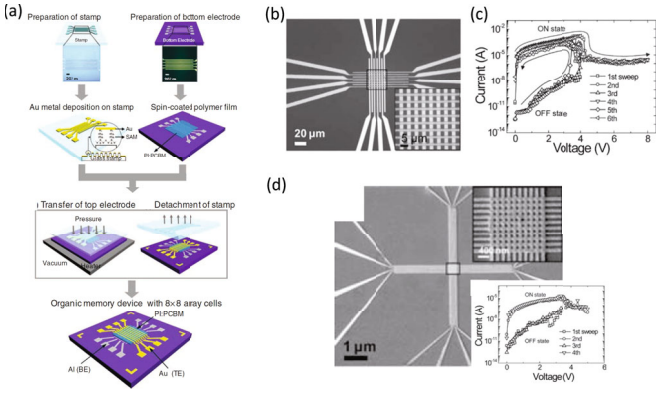

Fig. 4. (Color online) Direct metal transfer (2011) (a) Process flow of organic memory devices in an 8×8 array structure using DMT. (b) An optical image of the organic memory devices in a 2 μm-scale organic memory device (Al/PI:PCBM/Au). (c) I-V characteristics of 2 μm-scale organic memory device. (d) Scanning electron microscopy (SEM) image of 100 nm - scale organic memory devices in an 8×8 array structure. The inset shows I-V characteristics of 100 nm-scale organic memory device.

22]. Although these processes are good for pattern transfer, some methods require enormous printing pressure (several hundreds of MPa) for pattern transfer [19, 20]. Such high pressure may damage the active polymer layer. Kim *et al.* chose pattern transfer methods involving poly dimethyl siloxane (PDMS) stamps which employs low pressure and are useful due to its conformal contact at the interface between the stamp and the organic layer [23]. They reported on the fabrication of cross-bar type polymer non-volatile memory devices using a non-aqueous direct metal transfer (DMT) method with two-step thermal treatment. As an active memory polymer layer, WPF-oxy-F was used. Figure 3 shows a fabrication process for the direct metal transfer method. The first step is the preparation of a glass stamp. A transparent glass stamp with a linewidth of 2 μm was prepared *via* conventional photolithography and a subsequent etching process. Then, the glass stamp surface was deposited with a self-assembled monolayer as a releasing material (tridecafluoro-1,1,2,2-tetrahydroctyltrichlorosilane). An Au layer (35 nm) was deposited on the releasing layer to detach the metallic layer from the glass stamp easily, because it has poor adhesion against the releasing layer, and then a Ag layer (40 nm) was deposited on the Au layer using an electron beam evaporator. Prior to spin-coating of the active polymer layer, to remove the native oxide layer, the substrate was treated *via* a diluted HF-last process. Then, the solution of WPF-oxy-F dissolved in a mixture of methanol and water was spin-coated on the patterned substrates at 4000 rpm for 30 s, and the resulting thickness of the WPF-oxy-F film was measured to be around 100 nm. To improve film uniformity and to eliminate solvent from the film, post-baking was performed at 150 °C for 20 min on a hotplate prior to the DMT process for the top electrodes. The third step is to transfer the top electrodes by the DMT method. The metal deposited glass stamp was aligned at 90° to the bottom electrodes, and then pressed on the WPF-oxy-F layer, which as first heated to 100 °C with a pressure of 550 psi for 10 min. The final step is detaching the glass stamp. When the sample was cooled down to 80 °C, the glass stamp was detached from the polymer active layer. The Ag layer was transferred on the WPF-oxy-F layer by easy detachment of the Au layer from the stamp surface. In Fig. 3(b), the representative I-V curves of polymer memory devices fabricated by both the DMT and shadow mask methods. Both devices showed similar switching characteristics in spite of the different patterning methods. The device yield was 64% (42 out of 64 cells) in devices made by DMT method and 90% (60 out of 64 cells) in devices made by shadow mask methods, respectively. Figure 3(c) shows device uniformity in memory arrays fabricated by both methods. In the devices made by the conventional shadow mask method, the distributions of both the LRS and the HRS are within an order of magnitude, and the difference between the HRS and the LRS was still more than one order of magnitude, indicating reasonably good reversible switching characteristics for nonvolatile memory applications [23]. DMT method can be used in more soft condition (100 °C and 2 MPa).

Furthermore, Kim *et al.* demonstrated unipolar organic resistive memory devices scaled down to nanometer scale by DMT [24]. In this study they employed a hard glass stamp which enables the precisely shaped transferred pattern due to the conformal contact between the hard glass stamp and the substrate. A composite material consisting of polyimide (PI) and 6-phenyl-C61 butyric acid methyl ester (PCBM) was used as active

memory layer, which exhibits unipolar resistive switching characteristics. With similar process used by previous WPF-oxy-F memory made by DMT method, they fabricated unipolar organic resistive memory devices in cross-point architecture with 2 μm and 100 nm line widths. In the case of the organic memory devices with a 100 nm cell size, the bottom electrodes were prepared on the substrate by nanoimprint lithography, and the top electrodes were defined using DMT with a transparent stamp duplicated from a silicon master patterned by electron-beam lithography. Figure 4 shows device image and the *I-V* characteristics of the organic memory devices. Notably, in comparison with 2 μm-scale memory devices, a reduction in the ON current level was observed in the 100 nm-scale memory devices, which might be attributed to the decrease in the device area. The yield of the memory devices with 2 μm line width was 78% (50 out of 64 cells). They explained that switching failure in some cells seems to be attributed to the existence of non-uniform film thickness locally. While the yield of 100 nm scale memory device was poor. As scaling down the device to nanoscale, the device yield seemed to be strongly affected by the surface morphology of the surface. DMT method could miniaturize the organic resistive memory devices down to nm-scale with reasonably simple fabrication process [24]. However, it needs a perfect flat surface morphology, as incorporation of a planarization layer between the bottom electrodes to have a flat surface prior to the DMT process is scheduled, which would bring a complicated fabrication process in organic electronic devices.

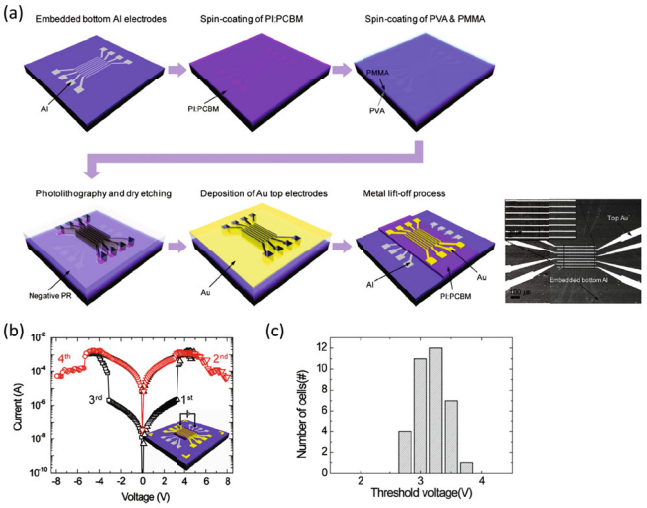

Fig. 5. (Color online) Conventional photolithography using buffer layer. (a) The fabrication of organic memory devicees with 8×8 arrays and embedded bottom electrodes using conventional photolithography. (b) The *I-V* characteristics of an Au/PI:PCBM/Al memory device. (c) A histogram of the threshold voltages.

4. Conventional photolithography with buffer layer

Although DMT method is cost-effective it was still not trivial to optimize the process conditions, which should differ depending on the organic materials used. With this regard, in 2012, Cho *et al.* demonstrated organic memory devices in an 8×8 crossbar array structure with electrode (4 μm line width) using conventional photolithography [25]. Fabrication involved a bilayer film of polymethyl methacrylate (PMMA)/polyvinyl alcohol (PVA) on top of the organic memory active layer, where PMMA functioned as buffer layer to prevent the dissolution of the PVA layer during developing process, and PVA acted as a layer actually striped during metal lift-off. Figure 5 shows the fabrication and electrical characterization of 8×8 crossbar array organic memory devices. With the use of positive photoresist, 8 trench lines were defined on a SiO_2/Si substrate, and approximately 50 nm of SiO_2 were then dry-etched using a reactive ion etching system. Al was deposited to fill the trench. After lift-off, embedded Al electrodes were constructed, which can make a smooth surface after PI:PCBM spin coating. PI:PCBM was used for the active memory layer. Before spin-coating with PI:PCBM, an O_2 plasma treatment was applied to the samples, which improved the adhesion and enhanced the switching reproducibility [26]. The thickness of PI:PCBM memory layer was about 25 nm. They reported that thinner organic film on the protruding bottom structures can make a bad step coverage so that embedded bottom electrodes are necessary for the memory devices [25]. The PI:PCBM layer is vulnerable to the developer used during photolithography. To avoid such damage to the active PI:PCBM layer, a PMMA/PVA bilayer film was inserted before the photoresist coating. A water-soluble PVA polymer was used as a layer actually stripped during subsequent metal lift-off because the cured PI:PCBM layer is relatively resistant to water. However, the PVA was only weakly resistant to the MIF 300 developer of the negative photoresist. To prevent damage to the PVA layer during the developing process, an approximately 100-nm-thick PMMA interlayer was inserted between the PVA and the photoresist. A negative photoresist was subsequently spin-coated onto the PMMA layer and was defined by 8 lines that followed by the dry etching of both the PMMA and PVA layers using O_2 plasma. This was followed by the dry etching of both the PMMA and PVA layers using O_2 plasma. As there was no etching selectivity between the two polymer layers, the etching process was performed based on etching rate of each layer for the time necessary for removing the two layers. In particular, a slow dry etching condition was selected to minimize the unwanted etching of the active PI:PCBM layer. The PVA layer then lifted off using DI water. Particularly, metal etching process could not be applied due to the limitation on the use of chlorine gas which is necessary for dry etching of Al metal. Fur-

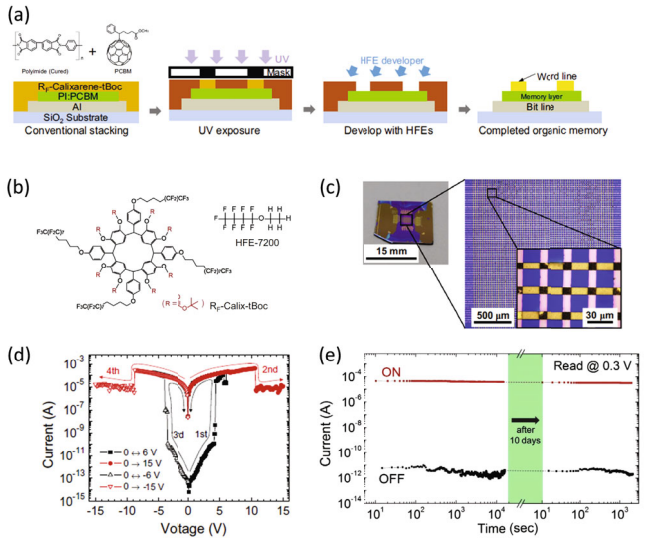

Fig. 6. (Color online) Orthogonal photolithography. (a) Schematics of fabrication of 4K-bit organic resistive memory devices. (b) Chemical structures of fluorinated photoresist and HFE-7200. (c) Optical images of the fabrication 4K-bit organic memory devices. (d) *I-V* characteristics of a memory cell with 10 μm size. (e) Retention test results for the 4K-bit organic memory devices.

thermore, by-products generated during the dry etching process are known to detrimentally influence the switching characteristics. Generally, the surface of the spin-coated PI:PCBM organic layer follows the morphology of the bottom electrodes patterned on the substrate, which determines the geometry of the cross-junction memory cell. Therefore, an embedded bottom electrode architecture would be more preferred in terms of switching reproducibility and reliability of such memory devices. The threshold voltages to writing the memory cells were distributed in a range between 2.5 and 4 V. Because the value of the threshold voltage is known to be related to the thickness of the active layer [27], accuracy in controlling the thickness of the PI:PCBM layer after dry etching was claimed to be critical. This method employs conventional photolithography by using buffer layer with aqueous solution. The PI:PCBM layer was susceptible to aqueous solution, however, a large portion of organic materials are vulnerable to hydrophilic solvent including aqueous solution. Besides, the advantage of easy fabrication of organic resistive memory is hindered by using extra buffer layer and etching process.

5. Orthogonal photolithography using fluorinated photoresist

The cross-bar structured organic memory devices have usually been limited to be less than a hundred bits integration with the individual cell size of several hundreds of microns. As mentioned above, the conventional photolithographic patterning technique to scale down the devices was considered to have problems with being applied to organic electronics due to the chemical incompatibility between organic electronic materials and organic solvents for photolithographic processing [28]. To overcome the lithographic problem in organic electronics, some research groups demonstrated a chemically non-damaging orthogonal photolithographic method that allows one to protect the underlying polymer organic films from the action of lithographic chemicals [29–33]. One possible solution was to adopt fluorinated photoresist and fluorinated solvents, which are miscible to each other and immiscible (orthogonal) to the most of other organic materials. These materials allowed organic electronic devices to be fabricated at the microscale using conventional photolithography process [29,31]. With this regard, Song *et al.* demonstrated the microfabrication of highly integrated 4,096-bit organic nonvolatile resistive memory devices with 10 μm × 10 μm cell size using orthogonal photolithography method [28]. Figure 6 shows the application of orthogonal photolithography on fabrication of organic memory devices. For the fluorinated photoresist solution, 10 wt% of semi-perfluoroalkyl resorcinarene powder and 0.5 wt% of N-nonafluorobutanesulfonyloxy-1,8-naphthalimide photoacid generator were dissolved into a mixed solvent (3-ethoxy-1,1,1,2,3,4,4,5,5,6,6,6-dodecafluoro-2trifluoromethylhexane (HFE-7500) : propylene glycol methyl ether acetate (PGMEA)= 4 : 1 weight ratio). For the active memory material, PI:PCBM was used. The 20-nm thick Al bottom electrode lines with 10 μm line width were fabricated using conventional photolithography. To enhance the film uniformity, the Al bottom electrodes were exposed to UV-ozone for 10 min. The prepared organic memory solution was spin coated onto the substrate, followed by hard baking. Then, the fluorinated photoresist solution was spin coated, followed by baking process at 75 °C for 3 min under yellow light. Subsequently, the coated photoresist film was exposed under UV light through a photomask with 10 μm lines. After post-exposure baking at 75 °C for 3 min, the photoresist film was developed by HFE-7200. Top electrodes of 30 nm-thick Au layer were deposited on the developed samples and lifted of in an ethanol mixture in HFE-7200 (5 vol%) to leave the patterned Au electrodes. Figure 6(c) shows optical images of the 4K-bit microscale organic memory devices with a memory cell size of 10 μm × 10 μm. The whole memory devices were integrated within 2 mm × 2 mm space. Another advantage to use fluorinated solvent such as HFE series was is that they are highly environmental and harmless to biological systems. As shown in Fig. 6(d), the microscale memory cell exhibited proper unipolar memory switching characteristics, which suggested that the memory devices fabricated by orthogonal photolithography properly operated without any damage by fluorinated chemicals. For a retention test, a microscale

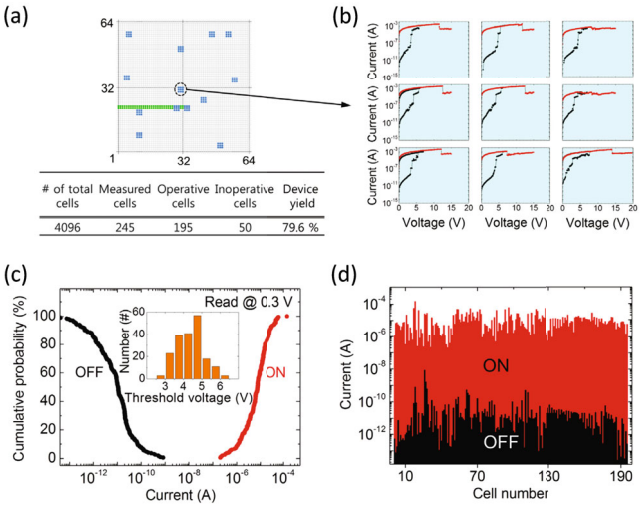

Fig. 7. (Color online) Orthogonal photolithography. (a) A schematic of the regions selected from a 4K-bit organic memory array and a table summarizing the device yield. (b) *I-V* curves measured from a selected region shown in (a). (c) Cumulative probability of on and off currents for all operative memory cells (195 cells) and the threshold voltage distribution (inset). (d) Representation of on and off currents of all operative memory cells.

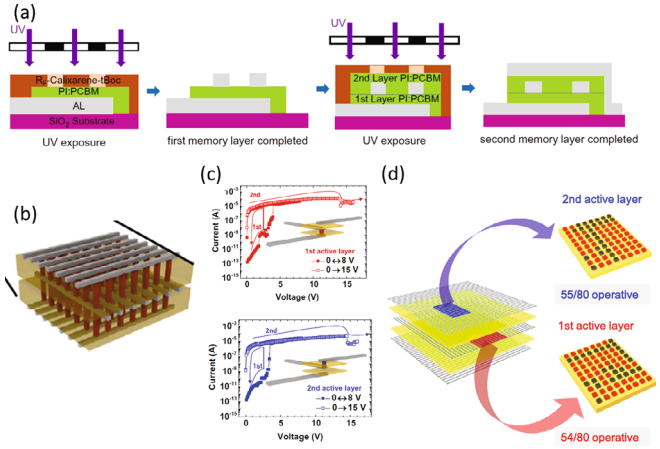

Fig. 8. (Color online) Vertical stacks using orthogonal photolithography. (a) Fabrication process of vertically stacked double layers of microscale organic memory devices. (b) a schematic illustration of the vertically stacked integration. (c) *I-V* curves of vertically stacked organic memory (d) Representation of device operation yield of the vertically stacked microscale organic memory devices.

organic resistive memory exhibited 10,000 s retention time with high on/off current ratio (10^7). Then, after 10 days of storage in a nitrogen environment, the same device was again subjected to retention test for 2,000 s and exhibited excellent retention property without any damage. Song *et al.* further showed the statistical characteristics of operation of highly integrated organic memory devices (Fig. 7) [28]. Figure 7(a) shows a table summarizing the yield of the memory devices as well as a schematic showing the regions of the memory cells that were sampled for measurement. Among 4,096 cells, a total of 245 cells were randomly selected and measured. Then 195 cells operated properly, corresponding to a device yield of $\sim$ 80%, which is relatively high yield value compared to other organic resistive memory devices. The device failures were attributed to uneven thickness of the organic layer and breakdown of electrodes or dielectric. To check the overall device operational uniformity, the current levels of the on and OFF states were statistically analyzed for the operative cells on a single chip (Fig. 7(c)). The memory devices showed a well-defined margin between the on/off current levels. Figure 7(d) displays the distribution of paired on/off current levels of each cell. The majority of the memory cells exhibited a large difference in order ($\sim 10^6$) between on and OFF states. Furthermore, Song *et al.* demonstrated a fabrication of organic memory devices on the flexible substrate (PET) [34]. To improve the density of the organic memory devices for the purpose of highly integrated device architecture, Yoo *et al.* fabricated vertically stacked microscale organic resistive memory devices [35]. The fabricated devices consisted of vertically stacked two layers of 32 $\times$ 32 crossbar-structured organic memory devices (total of 2,048 memory cells) with a memory cell size of 7 μm $\times$ 7 μm (Fig. 8). All the electrodes were selected to be Aluminum to avoid unnecessary fabrication process. Identical *I-V* characteristics between a first layer cell and a second layer cell indicated the successful vertical stacks of microscale organic resistive memory devices. Both first layer and second layer exhibited similar device operation yield of $\sim$ 70%. The application of orthogonal photolithography suggested breakthrough in ultrahigh integration of organic memory devices by enabling conventional photolithography without redundant fabrication process. However, the fluorinated photoresist should be further optimized to enhance its insensitivity to UV light intensity and surface roughness.

6. Miniaturization *via* nanostructure growth

As well as definition of microscale top electrodes is important for miniaturization of organic memory devices, miniaturization of organic memory layer itself is crucial for further high-density and stable memory modules. Ligorio *et al.* employed glancing angle deposition (GLAD) of organic materials to achieve laterally separated nanoscale organic molecular columns (Fig. 9) [36]. Directing the molecular beam under an oblique incident angle onto a substrate resulted in arrays of separated columnar nanostructures due to shadowing effects. GLAD method [37, 38] resulted in nanocolumns of the organic hole-transport material N,N'-di(1-naphthyl)-N',N'-diphenyl-(1,1'-biphenyl)-

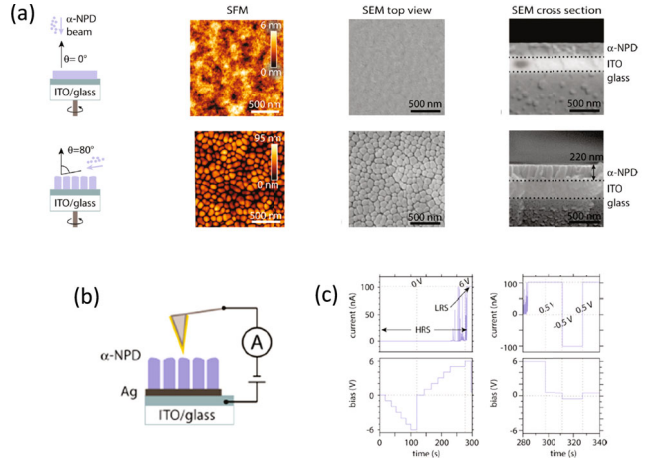

Fig. 9. (Color online) Glancing angle deposition. (a) Deposition geometry, SFM images, SEM top view images and SEM cross section images of normal incidence evaporation and GLAD evaporation. (b) Schematic diagram depicts the experimental setup during the electrical characterization *via* C-SFM of a nanocolumn grown on Ag. (c) Electrical switching properties of the memory device.

4,4'-diamine (α-NPD) with 100 nm diameter on a silver electrode. In their study, α-NPD exhibited bipolar switching characteristics which was attributed to the formation of metal filament due to the metal ion drift of reactive metal electrode [39–43]. With the conductive tip of a scanning force microscope (SFM), the top contact electrical characterization was performed as Au-coated conductive tip was brought into contact with the nano device. Normal angle deposition of α-NPD showed a continuous and featureless film on the ITO substrate. In contrast, cylindrically shaped columns were randomly distributed on the ITO substrate when setting angle to be 80° (GLAD). The nanocolumnar growth was explained to be a consequence of the evaporation under the condition of glancing angle and be amplified by Volmer-Weber or Stranski-Krastanov growth mode [38]. Surface outdents could represent nucleation points in a random ballistic process. With this shadowing effects, some nucleation points would shadow the neighbors. The nuclei, as result of the further evaporation of molecular vapor, would rise into columns normally oriented to the surface. To observe a resistance state change (switch to an on current state), it was necessary to use a reactive metal as an electrode, such as Ag (Fig. 9(e)). Figure 9(f) shows the applied bias and the measured current as a function of time. In reverse bias conditions, no current above noise level was measured, however, at forward bias, the current increased with sharp peaks during the stepwise increase of the bias (1 V step). In particular, a remarkable change of the current magnitude was observed at 6 V ($t \sim 270$ s). Subsequently lowering the bias to 0.5 V, the device still showed ON state. After biasing negative bias (−0.5 V), the current state went back to OFF state. Although realistic method for integration and operation should be further suggested related with the miniaturization *via* GLAD, this study is sufficiently meaningful because it suggested possibility of miniaturization of organic memory without complicated lithographic methods.

III. CONCLUSION

In summary, we have reviewed the development of techniques to miniaturize and integrate the organic resistive memory devices. Material characterization methods, stamping methods, etching methods, conventional photolithography method by using buffer layer or fluorinated photo resist and nanostructure growth methods have demonstrated bright possibility for high-integration of organic resistive memory devices. Still there are a lot of challenges to solve such as integration of memory devise with selective element (for example, one diode-one resistor or one transistor- one resistor structures) and integration of nano-sized memory devices. However, those miniaturization methods explained above have provided a compelling demonstration of many of the miniaturization and integration technology concepts to be realized.

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