ACS NANO
Cite This: ACS Nano 2018, 12, 7109−7116
www.acsnano.org

ARTICLE

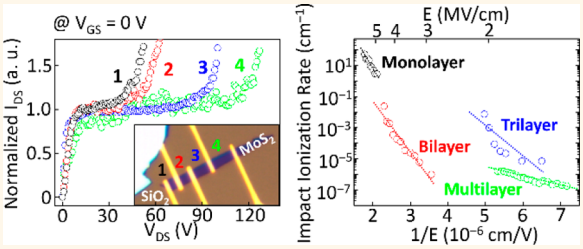
Two-Dimensional Thickness-Dependent Avalanche Breakdown Phenomena in MoS_2 Field-Effect Transistors under High Electric Fields

Jinsu Pak,[†,#] Yeonsik Jang,[†,#] Junghwan Byun,[‡] Kyungjune Cho,[†] Tae-Young Kim,[†] Jae-Keun Kim,[†] Barbara Yuri Choi,[†] Jiwon Shin,[†] Yongtaek Hong,[‡] Seungjun Chung,*[,§] and Takhee Lee*[,†]

[†]Department of Physics and Astronomy, and Institute of Applied Physics, Seoul National University, Seoul 08826, Korea
[‡]Department of Electrical and Computer Engineering, Inter-university Semiconductor Research Center (ISRC), Seoul National University, Seoul 08826, Korea
[§]Photo-electronic Hybrids Research Center, Korea Institute of Science and Technology (KIST), Seoul 02792, Korea

Supporting Information

ABSTRACT: As two-dimensional (2D) transition metal dichalcogenides electronic devices are scaled down to the sub-micrometer regime, the active layers of these materials are exposed to high lateral electric fields, resulting in electrical breakdown. In this regard, understanding the intrinsic nature in layer-stacked 2D semiconducting materials under high lateral electric fields is necessary for the reliable applications of their field-effect transistors. Here, we explore the electrical breakdown phenomena originating from avalanche multiplication in MoS_2 field-effect transistors with different layer thicknesses and channel lengths. Modulating the band structure and bandgap energy in MoS_2 allows the avalanche multiplication to be controlled by adjusting the number of stacking layers. This phenomenon could be observed in transition metal dichalcogenide semiconducting systems due to its quantum confinement effect on the band structure. The relationship between the critical electric field for avalanche breakdown and bandgap energy is well fitted to a power law curve in both monolayer and multilayer MoS_2.



KEYWORDS: *MoS_2, avalanche multiplication, 2D materials, field-effect transistors, electrical breakdown*

Ultrathin two-dimensional (2D) nanosheets of transition metal dichalcogenides (TMDs) have attracted much attention as post-silicon semiconducting materials because of their outstanding mechanical flexibility, transparency, and high surface to volume ratio and the absence of dangling bonds.[1−3] Among the TMDs, layered molybdenum disulfide (MoS_2) has been intensively researched due to its excellent electrical characteristics and thickness-dependent band structure (changing from an indirect energy bandgap of 1.2 eV to a direct bandgap of 1.8 eV as the number of layers decreases).[4−7] MoS_2 offers promising opportunities to realize emerging electronics, such as ultrathin transparent field-effect transistors (FETs),[8,9] logic circuits,[10,11] and sensor applications.[12−15] For use of MoS_2 in spatial integrated electronic design and applications, the channel length of FETs should be scaled down to sub-micrometer regimes. Consequently, it could be exposed to high lateral electric fields (*E*-fields), which can result in electrical breakdown. In addition, an electrical breakdown is affected by the electronic band structure and bandgap energy of semiconductors. Accordingly, the electrical breakdown in MoS_2 FETs will be determined by the thickness of the MoS_2 channel layer due to its quantum confinement, which allows the tunable band structure and bandgap energy. Therefore, a more thorough understanding of the origin of electrical breakdown in MoS_2 semiconducting systems under high *E*-fields is highly desirable. To date, however, very little has been reported on the electrical characterization of MoS_2 under high *E*-fields because the atomically thin MoS_2 channel layer shows a limited thermal energy dissipation capability, which leads to thermal breakdown.[16,17] Also, high thermal resistance of its insulating interface materials such as SiO_2 and polymer dielectrics accelerates this phenomenon.[18] For these reasons, most electrical measurements in MoS_2 FETs have been performed in the linear regime with low source−drain bias to prevent thermal breakdown by Joule heating.

Received: April 19, 2018
Accepted: June 27, 2018
Published: June 28, 2018

DOI: 10.1021/acsnano.8b02925
ACS Nano 2018, 12, 7109−7116

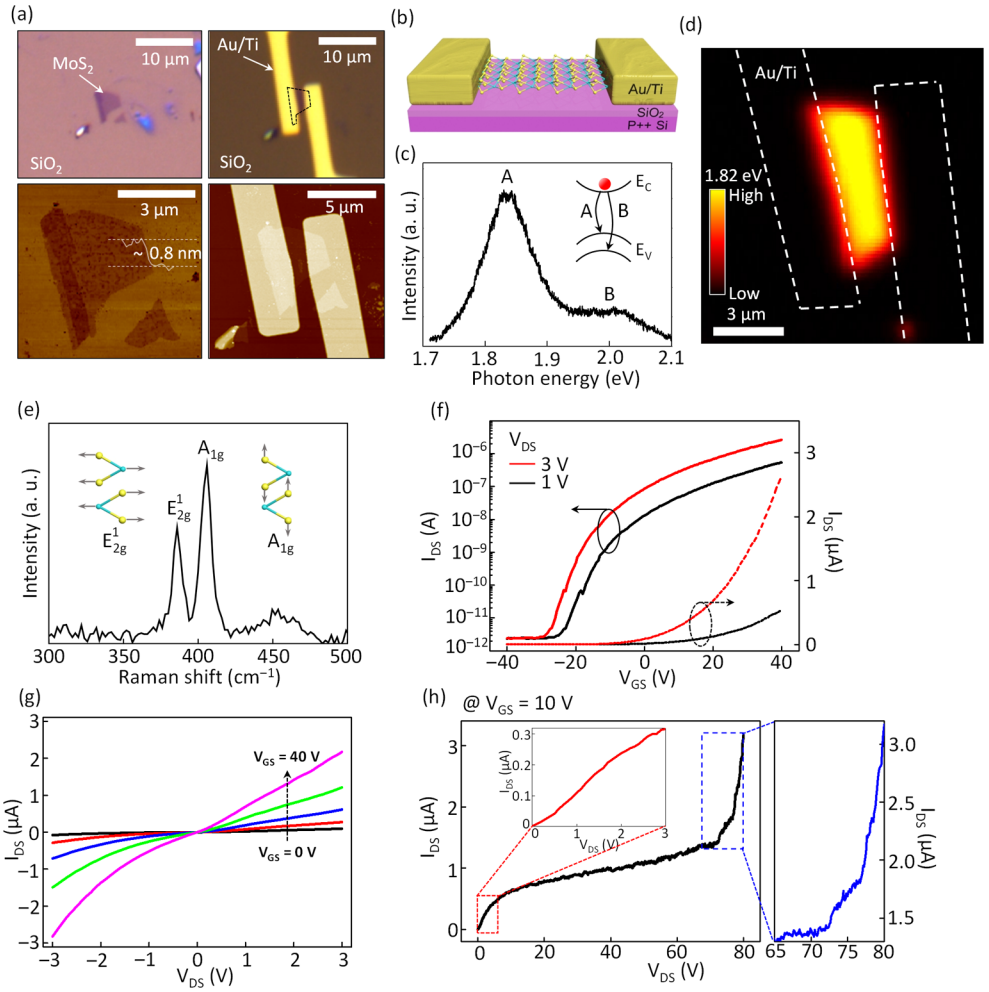


Figure 1. (a) Optical images (upper panels) and AFM images (lower panels) of a monolayer MoS_2 flake and fabricated MoS_2 FET. (b) Schematic of the fabricated MoS_2 FET with Au/Ti contacts. (c) PL spectra, (d) PL mapping image, and (e) Raman spectra of a mechanically exfoliated MoS_2 channel layer. (f) Representative transfer and (g) output curve of a monolayer MoS_2 FET. (h) Output curve exhibiting electrical breakdown in the high V_{DS} regime over 70 V. The I_{DS} increased linearly in low *E*-field regime (plotted with a red line), whereas it increased abruptly in the high *E*-field regime (plotted with a blue line).

Here, we studied the electrical breakdown in MoS_2 FETs with different bandgap energies using MoS_2 channels of different thicknesses. The observed electrical breakdown of MoS_2 FETs in high *E*-fields is attributed mainly to impact ionization in the MoS_2 channel, which is called avalanche multiplication. The critical electric field (E_{CR}) and impact ionization rate (α), which are defined as the minimum *E*-field needed for avalanche multiplication and the number of electron−hole pairs generated per unit distance traveled by a hot carrier, respectively, were carefully investigated in MoS_2 with different thicknesses. In particular, a strong dependence of E_{CR} and α on the thickness of the MoS_2 layer was closely related to its quantum confinement effect observed in 2D systems. Also, we performed thermal simulation with COMSOL Multiphysics to investigate the thermal effect by Joule heating and heat dissipation on the electrical breakdown. Although it is well known that the transport mechanism of MoS_2 is charge-hopping transport,[19] both monolayer and multilayer MoS_2 FETs in this work have E_{CR}−bandgap relationships similar to those of three-dimensional semiconductor FETs.

RESULTS AND DISCUSSION

Figure 1a shows the optical images (upper panels) and atomic force microscopy (AFM) images (lower panels) of a mechanically exfoliated monolayer MoS_2 flake and a fabricated MoS_2 FET. A schematic of the MoS_2 FET is shown in Figure 1b. Here, the back-gated MoS_2 FETs were fabricated on 270 nm thick SiO_2 grown on a heavily doped Si substrate (see Methods and Figure S1 in the Supporting Information for a detailed description of the fabrication process). The MoS_2 layer thickness (~0.8 nm) measured by AFM, photoluminescence (PL) spectra (Figure 1c), PL mapping exhibiting a uniform bandgap energy at 1.82 eV (Figure 1d), and Raman frequency difference (20 cm^{-1}) data (Figure 1e), indicate that the prepared MoS_2 channel layer was a uniform monolayer.[20,21] In Figure 1c, the positions of peaks A (~1.82 eV) and B (~2.0 eV) correspond to the direct band-to-band transitions with the energy split from the valence band by spin−orbital coupling.[21] In addition, with an increasing number of MoS_2 layers, the PL intensity of the peaks decreased, and the peak positions red-shifted, which was caused by the transition of the band structure from direct bandgap to indirect bandgap (see Figure S2 in the Supporting Information).[22]

DOI: 10.1021/acsnano.8b02925
ACS Nano 2018, 12, 7109−7116

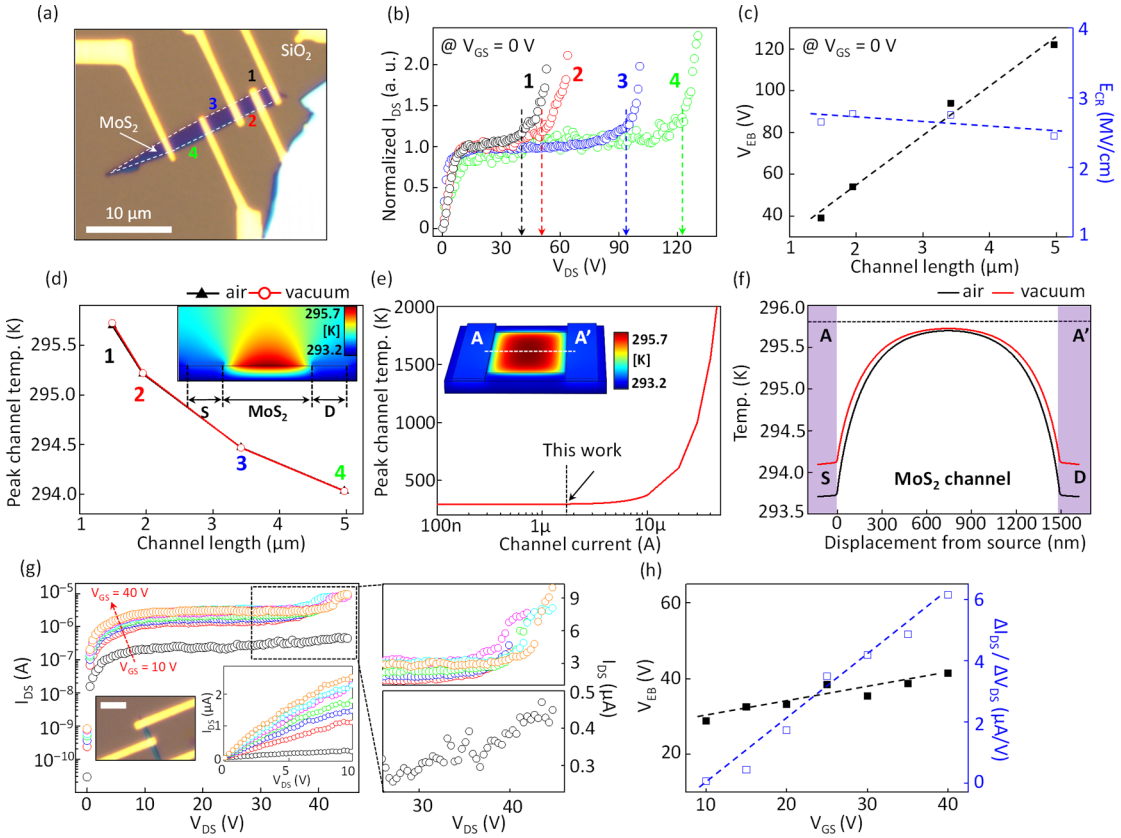


Figure 2. (a) Optical image of multilayer MoS_2 FETs (MoS_2 thickness of ~2.4 nm) with different channel lengths of 1.49, 1.95, 3.42, and 4.97 μm (labeled from 1 to 4, respectively) made on a common trilayer MoS_2 flake (thickness of ~2.4 nm). (b) Normalized I_{DS}–V_{DS} characteristics for the MoS_2 FETs measured at fixed V_{GS} = 0 V. Colored dashed lines indicate the breakdown voltages depending on the lateral *E*-fields. (c) V_{EB} and E_{CR} values *versus* the channel length of MoS_2 FETs, represented as black and blue symbols, respectively. (d) Peak channel temperatures corresponding to the MoS_2 FETs indicated in (a). An inset image shows a 2D thermal simulation result of the MoS_2 FET with a channel length of 1.49 μm. (e) Calculated peak MoS_2 channel temperature *versus* channel current in our device structure. An inset image indicates 3D thermal simulation result of the MoS_2 FET with a channel length of 1.49 μm. (f) Heat distribution of the MoS_2 channel along the dashed line in (e). (g) I_{DS}–V_{DS} characteristics at various gate voltages ranging from 10 to 40 V with a step of 5 V. An optical image of the multilayer MoS_2 FET is included in the inset (scale bar = 3 μm). (h) V_{EB} and $\Delta I_{DS}/\Delta V_{DS}$ values *versus* the gate voltage, represented as black and blue symbols, respectively.

Figure 1f and g show the transfer curve (*i.e.*, drain–source current *versus* gate voltage, I_{DS}–V_{GS}) and the output curve (*i.e.*, drain–source current *versus* drain voltage, I_{DS}–V_{DS}) of the monolayer MoS_2 FET measured in a vacuum (~10^{-4} Torr) at room temperature. Typical n-type semiconductor behaviors with an on/off current ratio over 10^7 were observed. The mobility (μ) of this representative device was determined to be 1.54 $cm^2/V{\cdot}s$, as calculated using the formula $\mu = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)\frac{L}{W}\frac{1}{C_i V_{DS}}$, with a channel length L = 1.6 μm, channel width W = 4.7 μm, and unit capacitance C_i = 13 nF/cm^2. From the I_{DS}–V_{GS} characteristics shown in Figure 1f, the transconductance ($G_m = dI_{DS}/dV_{GS}$) can be derived with different V_{DS} (see Figure S3 in the Supporting Information). As shown in Figure 1h, we clearly observed an abrupt increase of the channel current (measured at V_{GS} = 10 V) in the high V_{DS} regime (V_{DS} > 70 V), resulting in electrical breakdown. Note that this electrical breakdown was also observed in MoS_2 FETs with ohmic contacts, and most of the V_{DS} drop occurred across the MoS_2 channel layer, not at the contact region, due to the much higher channel resistance than the contact resistance. These results indicate that electrical breakdown was dominantly from the MoS_2 channel layer under high *E*-fields, not from the contact properties such as Schottky barriers (see Figures S4–S7 in the Supporting Information in detail). Also note that the electrical measurements were stopped before permanent device failures occurred by Joule heating, so reversible breakdown exhibiting abruptly increased current was observed during the multiple V_{DS} sweeps (see Figure S8 in the Supporting Information). The maximum current density of 1.72 × 10^6 A/cm^2 (maximum current divided by the channel width and MoS_2 channel thickness) at permanent breakdown in monolayer MoS_2 FETs and those of multilayer MoS_2 FETs are also presented in Figure S9 in the Supporting Information. The electrical characteristics, optical images, and scanning electron microscope (SEM) images of MoS_2 FETs after complete device failures are shown in Figures S10 and S11 in the Supporting Information. In general, there are three possible mechanisms for electrical breakdown in FETs: breakdown by drain-induced barrier lowering (DIBL), thermal runaway, and avalanche multiplication.[23] For these, it has been reported that a negligibly small DIBL (~10 mV/V) was observed in 2D semiconducting systems due to their excellent electrostatics, even for MoS_2 FETs with an extremely short channel length of 75 nm.[24] To explore the origin of the electrical breakdown in MoS_2 FETs, thorough investigations on MoS_2 FETs with different channel lengths, carrier concentrations, and bandgap

DOI: 10.1021/acsnano.8b02925
ACS Nano 2018, 12, 7109–7116

energies and in particular on the thermal effect by Joule heating are necessary.

To investigate the effect of lateral *E*-fields on the electrical breakdown, we fabricated MoS_2 FETs with various channel lengths (~1.49, 1.95, 3.42, and 4.97 μm) using a common trilayer MoS_2 flake (thickness of ~2.4 nm) (see Figure 2a). Note that the MoS_2 FETs had a uniform channel width of 2.2 μm. The electrical characteristics were measured in air. It should be noted that the adsorbed air molecules on MoS_2 damp down the vibration of the out-of-plane phonons, which leads to reduced energy loss by electron−phonon scattering. Therefore, the electrical breakdown can occur at lower breakdown voltages in air, as shown in Figure S12 in the Supporting Information. Examination of the normalized I_{DS}−V_{DS} characteristics shows that the initial voltages of electrical breakdown (V_{EB}), with an abrupt increase of the channel current, shifted to the positive V_{DS} direction as the channel length increased (see Figure 2b). Importantly, the values of V_{EB}, which are indicated with dashed lines, showed a linear relationship to the channel length (black symbols and dashed fitting line in Figure 2c). Then, the critical electric field (E_{CR}), which allows free electrons to have sufficient kinetic energy for creating electron−hole pairs (blue symbols and dashed fitting line in Figure 2c) of the MoS_2 FETs, was determined to be 2.66 MV/cm, on average, with a standard deviation of 0.15 MV/cm. The relationship between the channel resistivity and E_{CR} values also supports that this electrical breakdown was not dominantly originated by defects and adsorbates on the MoS_2 channel, as shown in Figure S13 in the Supporting Information.

To investigate the thermal effect by Joule heating on the electrical breakdown, the temperature increase and heat dissipation were analyzed with COMSOL Multiphysics. In this simulation, the dimensions of the FETs shown in Figure 2a were defined based on the measured dimensional parameters, and their electrical and thermal parameters were extracted from the measured electrical characteristics and from the literature (see Table S2 in the Supporting Information). Interestingly, the calculated peak temperatures caused by Joule heating of all the MoS_2 FETs in Figure 2a were too low to affect the device operation (peak temperatures *versus* the channel length are shown in Figure 2d). Note that due to the lower channel current in the long-channel device, the peak temperature on MoS_2 deceased as the channel length increased. This negligible temperature increase by Joule heating in the MoS_2 channel is attributed to the low channel current as shown in Figure 2e (a current range of ~μA when the electrical breakdown occurred). A previous research paper including the thermal simulation results by finite element modeling (FEM) reported that the temperature of the MoS_2 channel increased up to approximately its melting temperature at the channel current of a few milliamperes.[15] In our simulation model, it is consistent that the channel temperature also significantly increases over 1000 K if the channel current increases over 1 mA (see Figure S14 in the Supporting Information), but as aforementioned, microampere-range currents cannot generate a lot of heat that affects the electrical breakdown. In addition, we could not observe any physical damages by thermal effects on the MoS_2 channels after reversible electrical breakdown (see Figure S17 in the Supporting Information). Therefore, these results support that the electrical breakdown phenomena of MoS_2 FETs in high *E*-fields are primarily attributed to avalanche multiplication, not thermal effects by Joule heating. Furthermore, the reversible I_{DS}−V_{DS} behaviors including the electrical breakdown under the multiple V_{DS} sweeps at fixed V_{GS} also support that the MoS_2 channel was not damaged after the reversible electrical breakdown by thermal stress originating from Joule heating (see Figure S8 in the Supporting Information). Figure 2f shows the heat distribution in the MoS_2 FET (device 1 in Figure 2a) with the channel current of 1.8 μA at fixed gate bias (V_{GS} = 0 V). Due to the much higher thermal conductivity of the Ti/Au electrodes, the generated heat dissipated drastically near the contact regions, which indicates short-channel MoS_2 FETs have an advantage in relieving thermal stress *via* highly conductive contacts, although there is a trade-off with heat generation by the channel current. This result also indicates that the heat generated by Joule heating also increased the peak temperature of the contact region, but it could not be efficiently dissipated in a vacuum, resulting in the higher peak temperature at the contact regions in a vacuum compared to that calculated in air. Therefore, the temperature difference between the contact region and the channel region was relatively smaller in a vacuum compared to the case in air. Also, the dominant place of heat generation was located at the MoS_2 channel, not on the contact region, because the channel resistance was much higher than the contact resistance at fixed V_{GS} = 0 V (see Figures S14 and S15, Supporting Information). The design parameters and a measured value for the thermal simulations are summarized in Table S2 in the Supporting Information.

For further investigation, the effect of carrier concentration (which is modulated by gate electric field) on the abrupt increase of the channel current was investigated by adjusting the gate voltage. Figure 2g shows the I_{DS}−V_{DS} characteristics of a multilayer MoS_2 FET with a channel thickness of ~12 nm measured at various gate voltages ranging from 10 to 40 V, plotted on a semilogarithmic scale. We observed that V_{EB}, the starting point of the electrical breakdown, shifted in the positive drain−source voltage direction from 28.8 to 41.5 V as the gate voltage was increased (black symbols and dashed fitting line in Figure 2h). Corresponding E_{CR} values from 1.52 to 2.18 MV/cm are shown in Figure S18 in the Supporting Information. The origin of the higher V_{EB} is attributed to the increased electron−electron scattering with increasing accumulated carrier concentration in the MoS_2 channel (see Figure S19 in the Supporting Information). Therefore, a higher *E*-field is needed to observe electrical breakdown for compensating the energy loss by the electron−electron scattering. The increase of the gate bias also affects the number of generated electron−hole pairs such that the change of the channel current per unit drain−source voltage change ($\Delta I_{DS}/\Delta V_{DS}$) increases drastically, from 0.07 μA/V to 6.14 μA/V, when increasing the gate bias from 10 V to 40 V (blue symbols and dashed fitting line in Figure 2h). In other words, the electrical breakdown in the bias range over V_{EB} is accelerated proportionately with the number of free carriers. These results indicate that avalanche multiplication is the primary origin of the observed electrical breakdown of MoS_2 FETs in high *E*-fields. Note that if thermal runaway is the main mechanism for breakdown, then a larger current would produce an earlier breakdown phenomenon due to the Joule heating effect associated with a higher current, which is inconsistent with our observations (see Figure 2g).

The mechanism of avalanche multiplication is explained with the energy band diagram presented in Figure 3a. To generate

DOI: 10.1021/acsnano.8b02925
ACS Nano 2018, 12, 7109−7116

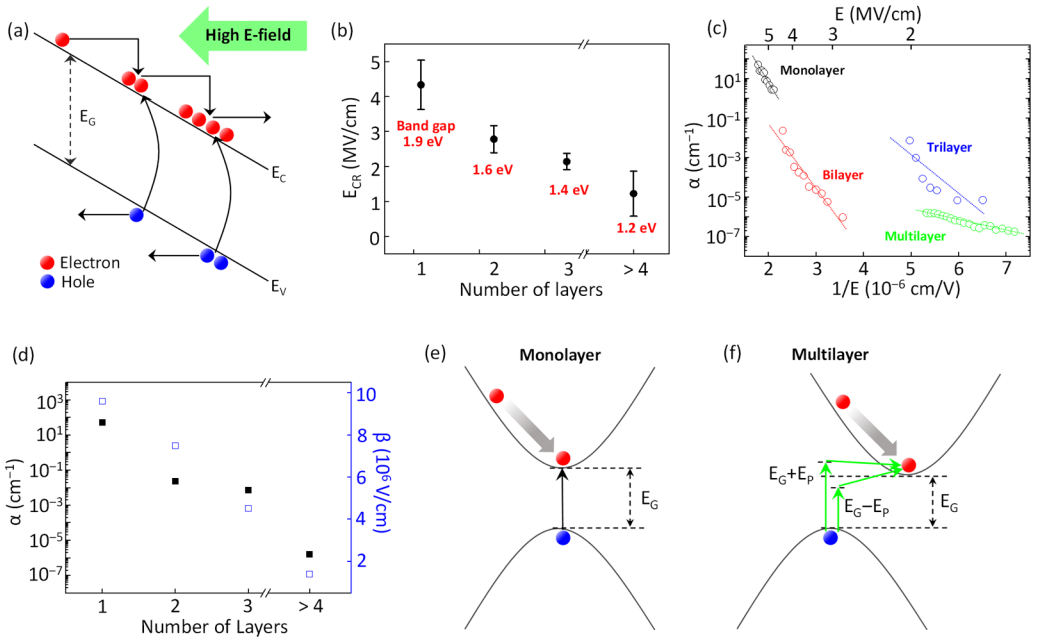


Figure 3. (a) Mechanism of avalanche multiplication phenomena. (b) E_{CR} values *versus* the number of MoS_2 layers. The error bars indicate the standard deviations of E_{CR} extracted from 3 to 7 different MoS_2 FET devices for each condition. (c) α values as a function of inverse *E*-field for the MoS_2 FETs with different numbers of MoS_2 layers. (d) Maximum α and calculated β values *versus* the number of layers of the MoS_2 channel, represented by black and blue symbols, respectively. Energy band structures for avalanche multiplication process in (e) monolayer and (f) multilayer MoS_2 FETs.

an electron−hole pair, free carriers should be accelerated with sufficient kinetic energy that can take out an electron from its bound state (in the valence band) to a state in the conduction band. Additionally, the generated electron−hole pair can be accelerated in high *E*-fields, and the pair can generate other electron−hole pairs. This process is called the avalanche multiplication or impact ionization process.[25] In this manner, a higher E_{CR} is needed to observe the avalanche multiplication for semiconductors with wider bandgaps. Therefore, we can expect that E_{CR} can be dependent on the number of MoS_2 layers (*i.e.*, MoS_2 film thickness) because MoS_2 has a layer-thickness-dependent bandgap energy. Note that in the avalanche multiplication in n-type semiconductors such as MoS_2, electron−hole pairs are generated mostly by accelerated electrons because of the larger impact ionization rate by an electron (α_e) than by a hole (α_h).[26]

Figure 3b summarizes the E_{CR} values for MoS_2 FETs with different MoS_2 layer thicknesses. For monolayer, bilayer, trilayer, and multilayer MoS_2 FETs, the E_{CR} was statistically determined as 4.33, 2.78, 2.14, and 1.22 MV/cm, respectively (representative I_{DS}−V_{DS} data are shown in Figure S20 in the Supporting Information). These *E*-field ranges are comparable with those in the previously reported studies on electrical characteristics of short-channel MoS_2 FETs (see Figure S21 in the Supporting Information). Note that the thickness of multilayer MoS_2 flakes ranged from 2.4 to 50.4 nm, corresponding to the variation from 4 layers to 72 layers. The E_{CR} decreased as the thickness of MoS_2 increased because the bandgap energy of MoS_2 increased with decreasing MoS_2 thickness, as shown in Figure 3b.

We investigated the impact ionization rate (α) expressed by the following equation:

$$\alpha = \frac{1}{n}\left(\frac{dn}{dx}\right) = \frac{1}{v_d}\left(\frac{1}{K}\right)\left(\frac{dK}{dt}\right) \quad (1)$$

where n, v_d, and K are the electron concentration, electron drift velocity, and surface current density, respectively (see Supporting Information for details). The α values for MoS_2 FETs with monolayer, bilayer, trilayer, and multilayer MoS_2 channels were extracted by observing the relationship between the channel current and time. Figure 3c shows the plot of α *versus* $1/E$ (E is electric field) for different layer thickness MoS_2 FETs. The results were fitted with a Shockley form, $\alpha = \alpha_0 \exp(-\beta/E)$, where α_0 and β denote the constant extracted by an extrapolation method and the ionization parameter depending on the local *E*-field, respectively.[27,28] Specifically, as the thickness of MoS_2 increased from monolayer to multilayers, the maximum α values decreased drastically from 52.5 cm^{-1} to 1.6 × 10^{-6} cm^{-1}, and the calculated β values decreased from 9.6 × 10^6 V/cm to 1.4 × 10^6 V/cm, as summarized in Figure 3d. The strong thickness-dependence of the α and β values in MoS_2 FETs can be explained through the energy band diagrams showing the energy band structure transition (indicated in Figure 3e and f). As shown in Figure 3e and f, the electron−hole pair can be created by a collision with a hot electron. The energy conservation equation for the avalanche multiplication in monolayer MoS_2 with a direct bandgap energy can be written as[29]

$$\frac{1}{2}m_i^* v_i^2 = E_G + \frac{1}{2}m_{e1}^* v_{e1}^2 + \frac{1}{2}m_{e2}^* v_{e2}^2 + \frac{1}{2}m_h^* v_h^2 \quad (2)$$

Here, E_G is the bandgap energy and $m^*_{i,e1,e2,h}$ are the effective masses of the incident electron before the collision (i), incident electron after the collision (e1), the created electron (e2), and the created hole (h), respectively. Similarly, $v_{i,e1,e2,h}$ are the velocities of the incident electron before the collision (i), incident electron after the collision (e1), the created electron (e2), and the created hole (h), respectively. Equation 2 means that only kinetic energy above the bandgap energy is sufficient for creating an electron−hole pair *via* impact ionization.

DOI: 10.1021/acsnano.8b02925
ACS Nano 2018, 12, 7109−7116

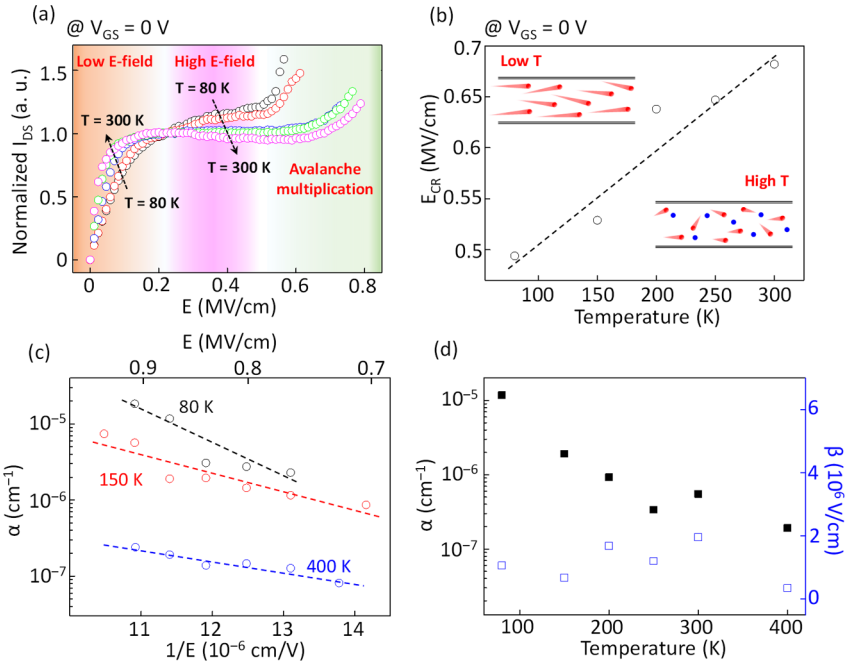


Figure 4. (a) Normalized I_{DS} as a function of E-field for various temperatures ranging from 80 to 300 K measured at V_{GS} = 0 V. (b) E_{CR} values depending on temperature extracted from the result of (a). (c) α values under different E-fields at various temperatures. (d) α and β values at different temperatures under a fixed E-field (0.88 MV/cm), represented by black and blue symbols, respectively.

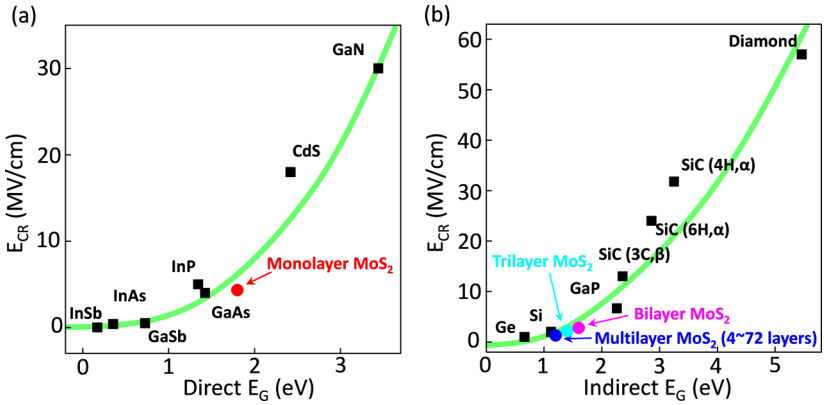


Figure 5. E_{CR} values for monolayer, bilayer, trilayer, and multilayer MoS_2 as well as those of conventional semiconductors. The solid green lines indicate that the E_{CR} of monolayer, bilayer, trilayer, and multilayer MoS_2 FETs were well-fitted to the given power law dependence of (a) $E_{CR} \propto E_G^{2.5}$ (direct bandgap) and (b) $E_{CR} \propto E_G^2$ (indirect bandgap). The E_{CR} values of the semiconductors were obtained from references: InSb,[31] InAs,[31] GaSb,[31] GaAs,[31] GaN,[31] Si,[31] SiC,[31] diamond,[31] InP,[33] CdS,[34] Ge,[35] and GaP.[36]

In contrast, as the number of MoS_2 layers increases, the conduction band minimum and valence band maximum become more separated in k-space (see Figure 3f). The energy conservation equation for avalanche multiplication in multilayer MoS_2 with an indirect bandgap energy is expressed as

$$\frac{1}{2}m_i^*v_i^2 = E_G \pm E_P + \frac{1}{2}m_{e1}^*v_{e1}^2 + \frac{1}{2}m_{e2}^*v_{e2}^2 + \frac{1}{2}m_h^*v_h^2 \quad (3)$$

Here, $\pm E_P$ denotes absorption and emission energies, respectively, of phonons with the wave vector equal to the wave vector difference between the created electron and hole (momentum conservation). Therefore, for multilayer MoS_2 FETs, the additional help of phonons is needed to create an electron−hole pair to fulfill both energy and momentum conservation, reducing the possibility of electron−hole pair creation. For this reason, the monolayer MoS_2 FETs showed higher α and β values than did multilayer MoS_2 FETs. These results indicate that avalanche multiplication in MoS_2 FETs is extremely sensitive to the number of MoS_2 layers corresponding to the thickness of the channel. Therefore, it is possible to easily optimize α and β values by adjusting the number of MoS_2 layers in MoS_2 applications exploiting avalanche multiplication.

We also measured I_{DS}−V_{DS} of a multilayer MoS_2 FET (~17 nm thick) at a fixed V_{GS} of 0 V under temperatures ranging from 80 to 300 K to investigate the effect of temperature on avalanche multiplication. As shown in Figure 4a, the normalized I_{DS} increased rapidly to its saturation current as the temperature increased in the low E-field regime because the thermal energy provided to the electron overcomes the Schottky barrier at the interface between the electrode and MoS_2 channel (see low E-field region in Figure 4a). In the high E-field regime, the electrons had sufficient energy to flow over the Schottky barrier and start to interact with optical phonons.

DOI: 10.1021/acsnano.8b02925
ACS Nano 2018, 12, 7109−7116

Therefore, the normalized I_{DS} decreased due to the energy loss caused by the scattering with optical phonons as temperature increases (see high E-field region in Figure 4a). The E_{CR} values at the start of avalanche multiplication were also sensitive to the temperature because a higher E-field was required to compensate for the energy loss by electron−phonon scattering as the temperature increased (Figure 4a and b). For the same reason, the α values were decreased significantly over 1 order of magnitude as the temperature increased from 80 K to 400 K in the entire E-field range (Figure 4c and d). These results strongly support the effect of temperature-dependent electron−phonon scattering on the electron−hole pair generation. Interestingly, the β values of multilayer MoS_2 were insensitive to temperature (open blue symbols in Figure 4d). This behavior is attributed to two compensating effects: a higher temperature increases electron−phonon scattering (negative effect for impact ionization) and reduces the bandgap energy of MoS_2,[30] leading to increased electron concentration (positive effect for impact ionization). The electrical characteristics of MoS_2 FETs under various temperatures ranging from 80 to 400 K and the E-field are described in detail in Figures S22 and S23 in the Supporting Information.

Because the bandgap structure and bandgap energy of MoS_2 are sensitively thickness-dependent, the key parameters of avalanche multiplication including E_{CR}, α, and β could be adjusted by its number of layers. It is well known that the E_{CR} is proportional to the bandgap energy to the power of 2.5 ($E_{CR} \propto E_G^{2.5}$) for direct-bandgap semiconductors, whereas the E_{CR} of indirect semiconductors is proportional to the square of the bandgap energy ($E_{CR} \propto E_G^2$).[31,32] Here, we compared the E_{CR} of MoS_2 FETs with the different number of layers to various conventional three-dimensional (3D) semiconductors. Figure 5a and b show that the E_{CR} values of monolayer MoS_2 with a direct-bandgap energy and multilayer MoS_2 (from 2 layers to 72 layers) with an indirect-bandgap energy were well fitted to the given power law dependences of $E_{CR} \propto E_G^{2.5}$ and $E_{CR} \propto E_G^2$, respectively. These results support that the avalanche multiplication phenomena observed in MoS_2 flakes are in good agreement with those of conventional 3D semiconductors and that their properties could be easily controlled by stacking the MoS_2 layers.

CONCLUSIONS

We investigated electrical breakdown phenomena in MoS_2 FETs under high E-fields. The effects of lateral E-fields and carrier concentration on the electrical breakdown indicated that avalanche multiplication is the origin of the electrical breakdown in MoS_2 FETs. The avalanche multiplication phenomena depended on the thickness of the MoS_2 channel layer. In particular, the E_{CR} and α of avalanche multiplication in MoS_2 FETs decreased with an increasing number of MoS_2 layers due to the thickness-dependent tunable band structure and bandgap energy of the 2D MoS_2 layers. The effect of electron−phonon scattering and the power law fitting of the relationship between E_{CR} and bandgap energy showed that the avalanche multiplication behaviors in MoS_2 were consistent with those in 3D semiconductors. Our study helps understand the electrical breakdown phenomena in MoS_2 under high E-fields. Furthermore, it will provide insight for the future achievement of controllable avalanche multiplication characteristics that are currently only feasible in thickness-dependent 2D layered MoS_2 and other transition metal dichalcogenides.

METHODS

Fabrication of MoS_2 FETs. To fabricate MoS_2 FETs, MoS_2 flakes were first transferred from a bulk MoS_2 crystal onto a 270 nm thick SiO_2/Si substrate using a micromechanical exfoliation method. On the transferred MoS_2, we spin-coated double electron resistor layers with methyl methacrylate (9% concentration in ethyl lactate) and poly(methyl methacrylate) 950 K (5% concentration in anisole) at 4000 rpm, sequentially. Each resist layer was baked at 180 °C for 90 s on a hot plate. The source and drain electrode patterns were defined by electron beam lithography (JSM-6510, JEOL), and Ti (5 nm) and Au (30 nm) layers were deposited using an electron beam evaporator (KVE-2004L, Korea Vacuum Tech.) sequentially for the source and drain electrode formation. The fabricated MoS_2 FETs were annealed at 200 °C in an Ar atmosphere for 2 h to achieve better electrical performances by eliminating the residues on the surface of the MoS_2 channels.

Electrical and Optical Characterization. The electrical properties of the MoS_2 FETs were measured using a semiconductor parameter analyzer (Keithley 4200-SCS) under various temperatures. Raman spectra, PL spectra, and PL mapping of MoS_2 were characterized using an XperRam 200 (Nanobase, Inc.) instrument with a 532 nm laser as the excitation source. The laser poser was 11.3 μW, with a diffraction-limited laser spot size (~1 μm spot radius).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.8b02925.

Details on MoS_2 FET fabrication, PL analysis depending on the thickness of MoS_2, transconductance of a monolayer MoS_2 FET, analysis on reversible electrical breakdown of MoS_2 FETs with different channel thicknesses and bias conditions, capacity of maximum current density per layer of MoS_2 FETs, permanent electrical breakdown in MoS_2 FETs, results of the thermal simulation using COMSOL Multiphysics, derivation of impact ionization rate, comparison of E_{CR} values in our work with those of other studies (PDF)

AUTHOR INFORMATION

Corresponding Authors

*E-mail: seungjun@kist.re.kr.
*E-mail: tlee@snu.ac.kr.

ORCID

Takhee Lee: 0000-0001-5988-5219

Author Contributions

#J. Pak and Y. Jang contributed equally to this work.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors appreciate the financial support of the National Creative Research Laboratory program (Grant No. 2012026372) through the National Research Foundation of Korea funded by the Korean Ministry of Science and ICT. J.H. and Y.H. appreciate the financial support of the R&D Convergence Program (CAP-15-04-KITECH) of Korean National Research Council of Science & Technology and the Technology Innovation Program (10041957) funded by the Korean Ministry of Trade, Industry and Energy. S.C. appreciates the support by the Korea Institute of Science and Technology (KIST) Future Resource Research Program (2E28310) and the National Research Foundation of Korea

DOI: 10.1021/acsnano.8b02925
ACS Nano 2018, 12, 7109−7116

grant (NRF-2017R1C1B2002323) funded by the Korean Ministry of Science and ICT.

REFERENCES

(1) Kim, S. J.; Choi, K.; Lee, B.; Kim, Y.; Hong, B. H. Materials for Flexible, Stretchable Electronics: Graphene and 2D Materials. *Annu. Rev. Mater. Res.* **2015**, *45*, 63−84.

(2) Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S. Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat. Nanotechnol.* **2012**, *7*, 699−712.

(3) Jariwala, D.; Sangwan, V. K.; Lauhon, L. J.; Marks, T. J.; Hersam, M. C. Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides. *ACS Nano* **2014**, *8*, 1102−1120.

(4) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS_2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147−150.

(5) Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F. Atomically Thin MoS_2: A New Direct-Gap Semiconductor. *Phys. Rev. Lett.* **2010**, *105*, 136805.

(6) Desai, S. B.; Madhvapathy, S. R.; Sachid, A. B.; Llinas, J. P.; Wang, Q.; Ahn, G. H.; Pitner, G.; Kim, M. J.; Bokor, J.; Hu, C.; Wong, H. -S. P.; Javey, A. MoS_2 Transistors with 1-Nanometer Gate Lengths. *Science* **2016**, *354*, 99−102.

(7) Yang, L.; Cui, X.; Zhang, J.; Wang, K.; Shen, M.; Zeng, S.; Dayeh, S. A.; Feng, L.; Xiang, B. Lattice Strain Effects on the Optical Properties of MoS_2 Nanosheets. *Sci. Rep.* **2014**, *4*, 5649.

(8) Lee, G.-H.; Yu, Y.-J.; Cui, X.; Petrone, N.; Lee, C.-H.; Choi, M. S.; Lee, D.-Y.; Lee, C.; Yoo, W. J.; Watanabe, K.; Taniguchi, T.; Nuckolls, C.; Kim, P.; Hone, J. Flexible and Transparent MoS_2 Field-Effect Transistors on Hexagonal Boron Nitride-Graphene Heterostructures. *ACS Nano* **2013**, *7*, 7931−7936.

(9) Yoon, J.; Park, W.; Bae, G.-Y.; Kim, Y.; Jang, H. S.; Hyun, Y.; Lim, S. K.; Kahng, Y. H.; Hong, W.-K.; Lee, B. H.; Ko, H. C. Highly Flexible and Transparent Multilayer MoS_2 Transistors with Graphene Electrodes. *Small* **2013**, *9*, 3295−3300.

(10) Wang, H.; Yu, L.; Lee, Y.-H.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L.-J.; Dubey, M.; Kong, J.; Palacios, T. Integrated Circuits Based on Bilayer MoS_2 Transistors. *Nano Lett.* **2012**, *12*, 4674−4680.

(11) Cheng, R.; Jiang, S.; Chen, Y.; Liu, Y.; Weiss, N.; Cheng, H.-C.; Wu, H.; Huang, Y.; Duan, X. Few-Layer Molybdenum Disulfide Transistors and Circuits for High-Speed Flexible Electronics. *Nat. Commun.* **2014**, *5*, 5143.

(12) Late, D. J.; Huang, Y.-K.; Liu, B.; Acharya, J.; Shirodkar, S. N.; Luo, J.; Yan, A.; Charles, D.; Waghmare, U. V.; Dravid, V. P.; Rao, C. N. R. Sensing Behavior of Atomically Thin-Layered MoS_2 Transistors. *ACS Nano* **2013**, *7*, 4879−4891.

(13) Kim, J.-S.; Yoo, H.-W.; Choi, H. O.; Jung, H.-T. Tunable Volatile Organic Compounds Sensor by Using Thiolated Ligand Conjugation on MoS_2. *Nano Lett.* **2014**, *14*, 5941−5947.

(14) Liu, B.; Chen, L.; Liu, G.; Abbas, A. N.; Fathi, M.; Zhou, C. High-Performance Chemical Sensing Using Schottky-Contacted Chemical Vapor Deposition Grown Monolayer MoS_2 Transistors. *ACS Nano* **2014**, *8*, 5304−5314.

(15) Gong, F.; Luo, W.; Wang, J.; Wang, P.; Fang, H.; Zheng, D.; Guo, N.; Wang, J.; Luo, M.; Ho, J. C.; Chen, X.; Lu, W.; Liao, L.; Hu, W. High-Sensitivity Floating-Gate Phototransistors Based on WS_2 and MoS_2. *Adv. Funct. Mater.* **2016**, *26*, 6084−6090.

(16) Lembke, D.; Kis, A. Breakdown of High-Performance Monolayer MoS_2 Transistors. *ACS Nano* **2012**, *6*, 10070−10075.

(17) Yang, R.; Wang, Z.; Feng, P. X.-L. Electrical Breakdown of Multilayer MoS_2 Field-Effect Transistors withThickness-Dependent Mobility. *Nanoscale* **2014**, *6*, 12383−12390.

(18) Yalon, E.; McClellan, C. J.; Smithe, K. K. H.; Rojo, M. M.; Xu, R. L.; Suryavanshi, S. V.; Gabourie, A. J.; Neumann, C. M.; Xiong, F.; Farimani, A. B.; Pop, E. Energy Dissipation in Monolayer MoS_2 Electronics. *Nano Lett.* **2017**, *17*, 3429−3433.

(19) Qiu, H.; Xu, T.; Wang, Z.; Ren, W.; Nan, H.; Ni, Z.; Chen, Q.; Yuan, S.; Miao, F.; Song, F.; Long, G.; Shi, Y.; Sun, L.; Wang, J.; Wang, X. Hopping Transport through Defect-Induced Localized States in Molybdenum Disulphide. *Nat. Commun.* **2013**, *4*, 2642.

(20) Li, H.; Zhang, Q.; Yap, C. C. R.; Tay, B. K.; Edwin, T. H. T.; Olivier, A.; Baillargeat, D. From Bulk to Monolayer MoS_2: Evolution of Raman Scattering. *Adv. Funct. Mater.* **2012**, *22*, 1385−1390.

(21) Splendiani, A.; Sun, L.; Zhang, Y.; Li, T.; Kim, J.; Chim, C.-Y.; Galli, G.; Wang, F. Emerging Photoluminescence in Monolayer MoS_2. *Nano Lett.* **2010**, *10*, 1271−1275.

(22) Dhakal, K. P.; Duong, D. L.; Lee, J.; Nam, H.; Kim, M.; Kan, M.; Lee, Y. H.; Kim, J. Confocal Absorption Spectral Imaging of MoS_2: Optical Transitions Depending on the Atomic Thickness of Intrinsic and Chemically Doped MoS_2. *Nanoscale* **2014**, *6*, 13028−13035.

(23) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*; John Wiley & Sons: Hoboken, 2007; pp 102−112.

(24) Yoon, Y.; Ganapathi, K.; Salahuddin, S. How Good Can Monolayer MoS_2 Transistors Be ? *Nano Lett.* **2011**, *11*, 3768−3773.

(25) Levinshtein, M.; Kostamovaara, J.; Vainshtein, S. *Breakdown Phenomena in Semiconductors and Semiconductor Devices*; World Scientific Publishing Co.: Singapore, 2005; pp 921−936.

(26) Lee, C. A.; Logan, R. A.; Batdorf, R. L.; Kleimack, J. J.; Wiegmann, W. Ionization Rates of Holes and Electrons in Silicon. *Phys. Rev.* **1964**, *134*, A761.

(27) Shichijo, H.; Hess, K. Band-Structure-Dependent Transport and Impact Ionization in GaAs. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1981**, *23*, 4197.

(28) Dalal, V. L. Avalanche Multiplication in Bulk n-Si. *Appl. Phys. Lett.* **1969**, *15*, 379.

(29) Sze, S. M.; Lee, M.-K. *Semiconductor Devices Physics and Technology*; John Wiley & Sons: Hoboken, 2012; pp 73−76.

(30) Plechinger, G.; Mann, J.; Preciado, E.; Barroso, D.; Nguyen, A.; Eroms, J.; Schüller, C.; Bartels, L.; Korn, T. A Direct Comparison of CVD-Grown and Exfoliated MoS_2 Using Optical Spectroscopy. *Semicond. Sci. Technol.* **2014**, *29*, 064008.

(31) Hudgins, J. L.; Simin, G. S.; Santi, E.; Khan, M. A. An Assessment of Wide Bandgap Semiconductors for Power Devices. *IEEE Trans. Power Electon.* **2003**, *18*, 907−914.

(32) Hudgins, J. L. Wide and Narrow Bandgap Semiconductors for Power Electronics: A New Valuation. *J. Electron. Mater.* **2003**, *32*, 471−477.

(33) Cook, L. W.; Bulman, G. E.; Stillman, G. E. Electron and Hole Impact Ionization Coefficients in InP Determined by Photomultiplication Measurements. *Appl. Phys. Lett.* **1982**, *40*, 589.

(34) Williams, R. High Electric Fields in Cadmium Sulfide: Field-Effect Constriction of Current Flow and Dieletric Breakdown. *Phys. Rev.* **1961**, *123*, 1645.

(35) Mckay, K. G.; Mcafee, K. B. Electron Multiplication in Silicon and Germanium. *Phys. Rev.* **1953**, *91*, 1079.

(36) Logan, R. A.; Chynoweth, A. G. Charge Multiplication in GaP pn Junctions. *J. Appl. Phys.* **1962**, *33*, 1649.

DOI: 10.1021/acsnano.8b02925
ACS Nano 2018, 12, 7109−7116