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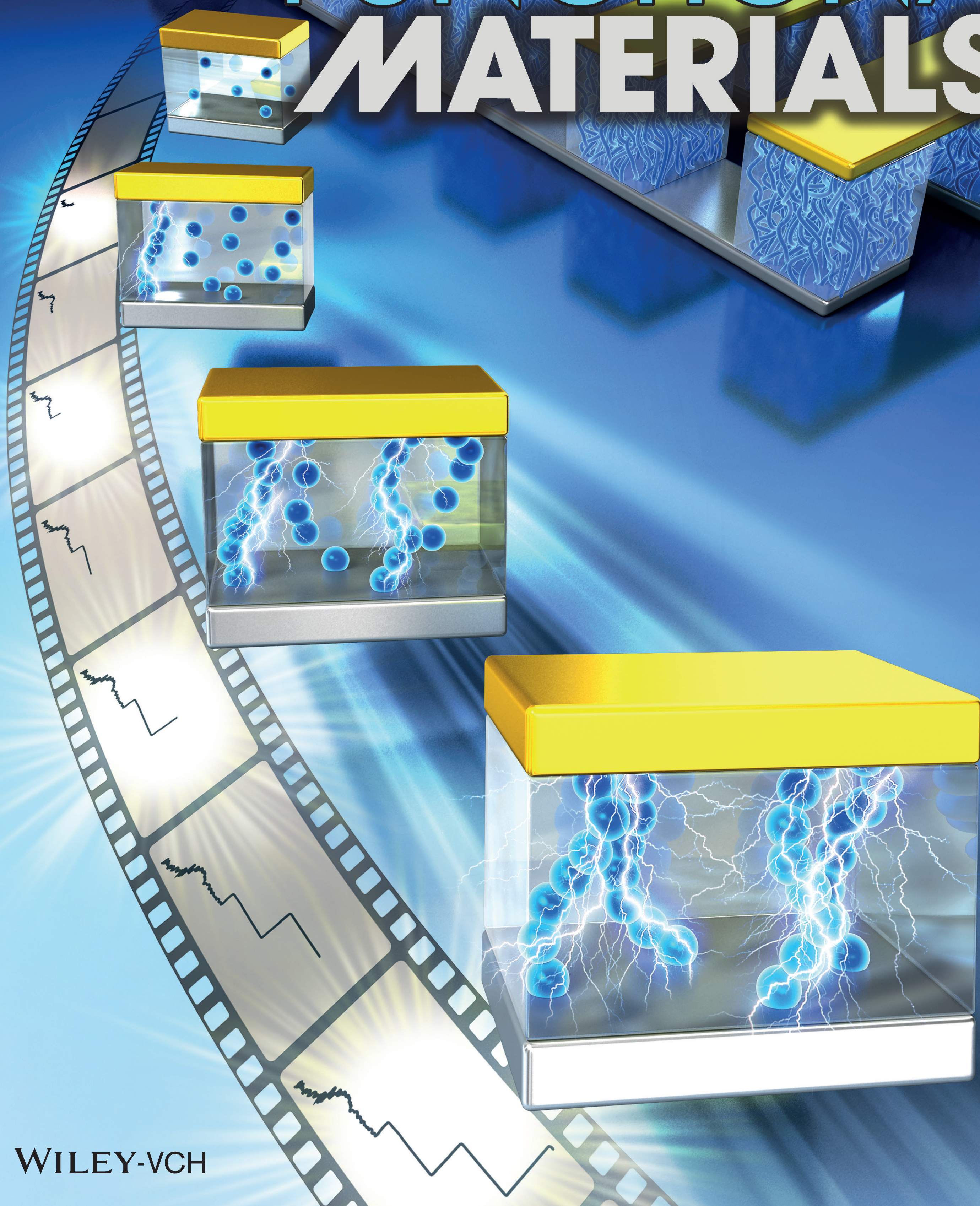

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Investigation of Time–Dependent Resistive Switching Behaviors of Unipolar Nonvolatile Organic Memory Devices

Woocheol Lee, Youngrok Kim, Younggul Song, Kyungjune Cho, Daekyoung Yoo, Heebeom Ahn, Keehoon Kang, and Takhee Lee**

Organic resistive memory devices are one of the promising next-generation data storage technologies which can potentially enable low-cost printable and flexible memory devices. Despite a substantial development of the field, the mechanism of the resistive switching phenomenon in organic resistive memory devices has not been clearly understood. Here, the time–dependent current behavior of unipolar organic resistive memory devices under a constant voltage stress to investigate the turn-on process is studied. The turn-on process is discovered to occur probabilistically through a series of abrupt increases in the current, each of which can be associated with new conducting paths formation. The measured turn-on time values can be collectively described with the Weibull distribution which reveals the properties of the percolated conducting paths. Both the shape of the network and the current path formation rate are significantly affected by the stress voltage. A general probabilistic nature of the percolated conducting path formation during the turn-on process is demonstrated among unipolar memory devices made of various materials. The results of this study are also highly relevant for practical operations of the resistive memory devices since the guidelines for time-widths and magnitudes of voltage pulses required for writing and reading operation can be potentially set.

1. Introduction

Organic materials for electronic devices have attracted great attention due to their advantageous properties such as material variety, low production cost, mechanical flexibility, and large area processing capability.[1,2] Among various organic electronic devices, organic nonvolatile resistive memory is one of the actively researched areas.

The organic resistive random access memory (ORRAM) devices can be realized by sandwiching various organic materials between the top and bottom electrodes in a vertical two-terminal structure.[3,4] The ORRAM devices possess at least two stable resistance states which can be switched to each other by an external electric field. ORRAM can be categorized according to the polarity of the switching electric field: unipolar memory devices which can be switched ON and OFF by applying the electric field in the same polarity and bipolar memory devices which require the electric field in the opposite polarities for the ON and OFF switching. Through extensive studies by many research groups, the electrical performances of ORRAM devices have been significantly improved along with advancement of architectural design and integration.[5–10] Nevertheless, the memory operation mechanism of ORRAM is still not completely understood. Especially, the operating principles of unipolar ORRAM devices which show S-shape current–voltage characteristics with a negative differential resistance (NDR) region are still controversial.[11–13]

Various experimental tools have been employed to investigate the fundamental properties of ORRAM devices; for example, impedance spectroscopy[12] to directly probe the charge trapping in the active layer and a direct spatial mapping of the current paths within the layer via elemental analysis.[14,15] We have recently employed $1/f$ noise measurements to show that the conduction paths in organic nanocomposite memory devices form a percolation network from the resistance scaling of the $1/f$ noise.[13,16] A further study of time–dependent current fluctuation behaviors during the turn-off process in the NDR region demonstrated that the percolating conduction paths dynamically changed before completely getting disconnected (i.e., OFF state).[13,16] However, there has been little research conducted on the formation process of this percolation network during the turn-on process.

In this study, we investigated the time–dependent resistive switching behaviors, especially in the turn-on process. We observed how the current in the device increased with time while applying a constant voltage stress for ORRAM devices that were made of a nanocomposite layer of polystyrene (PS) and phenyl-C61-butyric acid methyl ester (PCBM). The fundamental properties of the PS:PCBM ORRAM devices were

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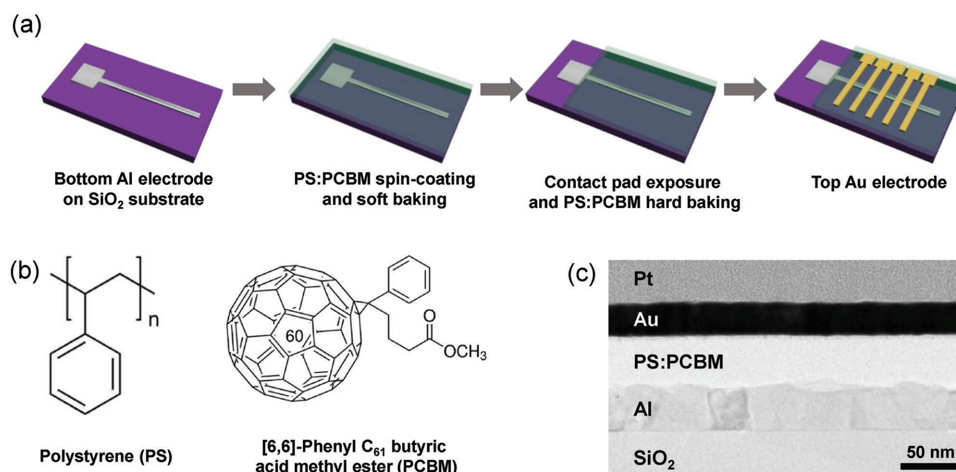

Figure 1. a) A schematic showing the device fabrication processes for Al/PS:PCBM/Au organic resistive memory devices. b) The molecular structure of the PS:PCBM composite material. c) A cross-sectional TEM image of the memory device.

revealed through a statistical analysis of the turn-on time values from multiple measurements by employing the Weibull distribution[17] which has been widely used for describing the electrical breakdown of various materials.[18–22] Our study is the first attempt of applying the Weibull statistics in the context of ORRAM devices, to the best of our knowledge. We compared the results for the PS:PCBM ORRAM devices with other devices made from three different organic and inorganic materials, and we extracted some common fundamental properties among the unipolar resistive memory devices.

2. Results and Discussion

Figure 1a shows the fabrication process of the ORRAM devices. First, Al (30 nm thick) was deposited as the bottom electrode on a SiO_2/Si substrate using a thermal evaporator. Then, a composite solution made with PS:PCBM dissolved in chlorobenzene was spin coated to form the memory layer (see Figure 1b). After a soft-baking of the samples, the contact pads of the Al bottom electrodes were exposed by sobbing with an acetone-soaked Q-tip cotton swab. After a hard-baking of the samples on a hot plate at 120 °C for 60 min, Au (30 nm thick) was deposited on the top electrodes. As a result, memory cells with a size of 100 µm × 100 µm were fabricated (see the Experimental Section for more details). Figure 1c shows the cross-sectional transmission electron microscope (TEM) image of a memory cell, indicating a well-defined PS:PCBM memory layer with a thickness of ≈40 nm, without any noticeable penetration of metals (Au and Al) into the layer.

The memory devices showed a typical unipolar behavior with the NDR. **Figure 2**a shows a representative current–voltage (I–V) curve of a PS:PCBM ORRAM device. The SET process consisted of sequential forward and reverse voltage scans between 0 and 5 V. Note that the bottom Al electrode was grounded and a bias voltage was applied at the top Au electrode. The resistive state changed from a high resistance state (HRS; OFF state) to a low resistance state (LRS; ON state) at the threshold voltage in a range of 3–4 V during the voltage sweep in the SET process. The LRS was maintained even when the applied voltage was removed, exhibiting nonvolatile memory characteristics. The RESET process consisted of a single voltage sweep from 0 to 12 V, in which the current decreased after ≈4 V and showed the NDR behavior. When the applied voltage was

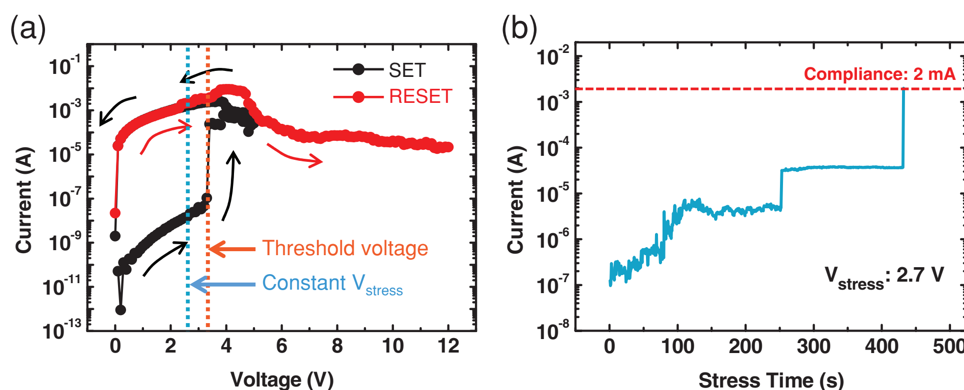

Figure 2. a) A representative current–voltage graph of a PS:PCBM memory device. b) A representative current–stress time curve under a constant voltage stress, V_{stress}, of 2.7 V.

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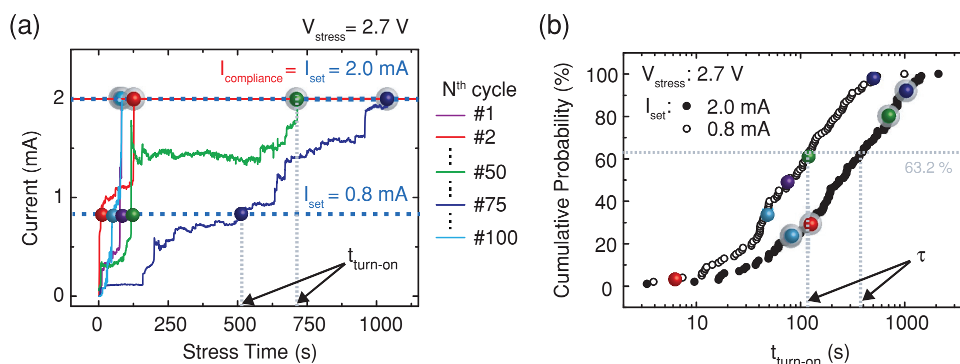

Figure 3. a) Selected current–stress time curves from 100 cycles (shown as different colors) of time-dependent current measurements in the same device under V_{stress} of 2.7 V. I_{set} was chosen as a reference current value for the device in the ON state. The time taken for the device current to reach I_{set}, $t_{turn\text{-}on}$, were read from the points represented as the circular marks for each I_{set} of 0.8 mA (circles) and 2.0 mA (shadowed circles). b) The cumulative probability of the time taken for the device current to reach $I_{set,}t_{turn\text{-}on}$, under V_{stress} of 2.7 V with I_{set} of 0.8 and 2.0 mA (see the circular marks in (a) for the corresponding data). The horizontal dotted line of 63.2% can be used to read characteristic times, τ.

removed at around 12 V, the memory device turned back to HRS. The memory devices could endure over 500 cycles of ON/OFF switching cycles and maintain the memory states for longer than 10^4 s (see Figure S1, Supporting Information, for more details).

Generally, to turn the memory devices from the HRS to LRS, a voltage pulse with the magnitude above a certain voltage is applied. Threshold voltage is commonly determined as a voltage at which the current abruptly increases in the current–voltage sweep scans. When memory devices are operated in the voltage pulse mode, a certain duration of voltage pulse is required to turn on the memory devices. In our previous study, we observed that the smaller the applied voltage, the longer the minimum time required to turn on the memory devices.[23] Here, one may expect that the turn-on process could occur even when the applied voltage is below the threshold voltage, provided that one applies the voltage for a long enough time. Thus, we measured the current over time while applying a constant voltage stress (V_{stress}) of an arbitrarily chosen value of 2.7 V (below the threshold voltage; see Figure 2a). We observed that the current under V_{stress} irregularly increased with several steps over time (see Figure 2b). After several step increases, the current ultimately reached 2.0 mA (set as the compliance) which is the expected current of ON state.

After the current reached the compliance, the RESET process described above was conducted to confirm the reversibility of the switching event. The memory device showed the same *I*–*V* curve of the RESET process shown in Figure 2a and turned off (see Figure S2b, Supporting Information). This means that the state of the memory device could change from the OFF to ON state under V_{stress} below the threshold voltage and that this process is effectively the same as the SET process. Here, we could infer that the threshold voltage is not a fixed value but is a variable that depends on the voltage stress-time.

The current steps revealed the existence of multiple intermediate resistive states (IRSs) before reaching the ON state. In order to check the stability of the IRS, we manually removed the stress voltage while at the IRS. We found that the IRS was stable and that the resistance value of the IRS corresponded to the value just before the stress voltage was removed (see Figure S2, Supporting Information).

We repeated the measurement shown in Figure 2b in multiple cycles while applying the same V_{stress} of 2.7 V in the same device to investigate the statistical relevance of the results, as shown in **Figure 3**a. All the current curves increased stepwise; however, the time difference between the steps and the height of the steps were all different. In some cycles, the current reached the compliance in a few seconds, whereas in other cycles, the current reached the compliance after 1000 s. Also, in some cycles, the current reached the compliance in one current step, while other cycles showed several current steps before reaching the compliance. Therefore, the turn-on time values have a finite distribution which indicates a probabilistic nature of the turn-on process. This means that the device does not turn on deterministically after a specific voltage or energy requirement is met.[23] It is also obvious that the turn-on process occurs through discrete events in which the current abruptly changes. The percolation conducting path models[13,16] may explain the experimental results above. Every step increase in the current may represent a new current path formation. Each current path has a different resistance, which is reflected in the different heights of the current steps.

For a deeper understanding of the turn-on process, we collected the time, $t_{turn\text{-}on}$, taken to reach a specific current value, I_{set} (see Figure 3a), by conducting the same measurements for different V_{stress}. We ran 100 measurement cycles for different V_{stress} varying from 2.7 to 3.2 V with an interval of 0.1 V and we read $t_{turn\text{-}on}$ values for six different I_{set} values of 0.2, 0.4, 0.8, 1.2, 1.6, and 2.0 mA. Figure 3b shows two representative cumulative probability graphs of $t_{turn\text{-}on}$ values which were measured at V_{stress} of 2.7 V and I_{set} of 0.8 and 2.0 mA. The two graphs look similar, but the graph for I_{set} of 0.8 mA shifted to the smaller $t_{turn\text{-}on}$ direction compared to the graph for 2.0 mA. This is because if one sets a smaller I_{set}, the memory device will reach the ON state earlier at a given V_{stress}. A complete data set of cumulative probability distributions for different V_{stress} and I_{set} values can be found in Figures S3 and S4 (Supporting Information). Note that we observed no significant device degradation throughout the cycles because $t_{turn\text{-}on}$ showed no dependence on the number of cycles. For example, the $t_{turn\text{-}on}$ for the second cycle was ≈120 s, whereas the $t_{turn\text{-}on}$ for the 50th and the 100th cycles was ≈700 and ≈100 s, respectively (see Figure 3a,b). The

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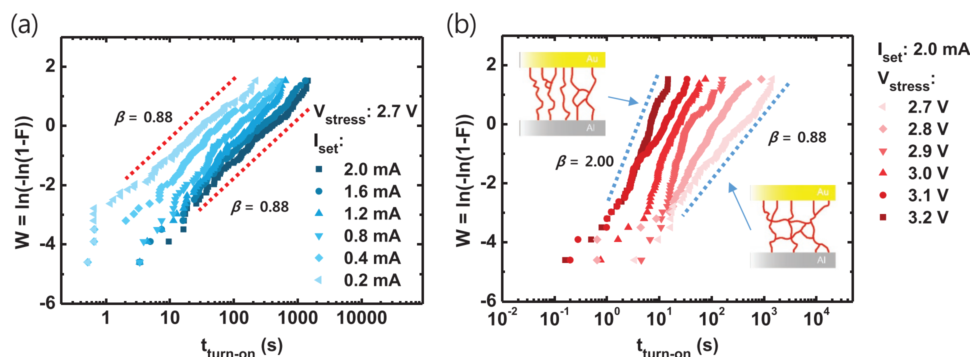

Figure 4. A linear fitting for the Weibull plots of $t_{turn\text{-}on}$ a) under V_{stress} of 2.7 V with six different I_{set} and b) under six different V_{stress} with I_{set} of 2.0 mA. The slopes of the fitted lines indicate the shape parameter, β, of the Weibull distribution. The insets in (b) are schematic representation of different networks of the current paths formed under different V_{stress}.

probabilistic nature of the time–dependent switching event can be analyzed by fitting the distribution of $t_{turn\text{-}on}$ values with the Weibull distribution. The Weibull distribution is one of the extreme value distributions[24] which has been widely used as an empirical law for describing the electrical breakdown phenomenon of a variety of insulators ranging from oxides to polymers via percolation leakage paths.[18–22] The following equation relates the cumulative probability of $t_{turn\text{-}on}$ according to the Weibull distribution

$$F(t) = 1 - \exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right) \quad (1)$$

where β is the shape parameter and τ is the characteristic turn-on time. In order to assess whether our experimental data follow the Weibull distribution, we plotted a linearized form of F, defined as $W = \ln(-\ln(1-F))$ as a function of $t_{turn\text{-}on}$. **Figure 4**a,b shows that the plots of $t_{turn\text{-}on}$ values for various I_{set} (under a constant V_{stress}) and for various V_{stress} (under a constant I_{set}) can all be fitted linearly. The slopes of these linear lines represent β which is related to the width of the distribution of $t_{turn\text{-}on}$, i.e., a larger β represents a narrower distribution of $t_{turn\text{-}on}$ for a given τ.

We investigated the physical meaning of β and τ in the switching process by analyzing their dependence on V_{stress} and I_{set}. Figure 4a shows that β has a little dependence on I_{set} since the lines for different I_{set} were fitted linearly with similar slopes (shown explicitly in Figure S5a, Supporting Information). On the other hand, β changed depending on V_{stress}; β increased as V_{stress} increased (Figure 4b). The fitted β varied from 0.88 at V_{stress} of 2.7 V to 2.00 at 3.2 V. A complete set of data for β at different V_{stress} and I_{set} is shown in Figure S5 (Supporting Information). The change of β with respect to V_{stress} may indicate the nature of the resistive switching process in the memory devices. The best analogy can be taken from the percolation model for an electrical breakdown in insulating polymers,[19,25,26] which has been explained as either a percolation-like breakdown or a filamentary-like breakdown.[27,28] The insets of Figure 4b show the schematics that represent two different resulting networks of the device in LRS. The percolation current path formation may have a preferred direction of formation according to the direction of the applied electric field. When V_{stress} becomes larger, the percolation current path formation is more directional along the field, which would tend to form more localized current paths. This is reflected in the higher value of β at larger V_{stress}.

We now investigate the physical meaning of τ by analyzing its dependence on V_{stress} and I_{set}. τ is calculated from the linear fitting of the linearized Weibull distribution plot in Figure 4a according to Equation (1). **Figure 5**a shows how τ changes with I_{set} under different V_{stress}. Obviously, the larger the I_{set}, the larger the τ. The relationship between τ and I_{set} seems linear. Note that τ is a representative value of $t_{turn\text{-}on}$, which is the value at 63.2% in the cumulative distribution of $t_{turn\text{-}on}$. The τ values are indicated by the arrows in Figure 3b. τ could be considered similar to the mean value of all $t_{turn\text{-}on}$ values. The apparent relationship between τ and I_{set} indicates that the irregular current increases observed in Figure 3a are not completely random but follow a particular statistical behavior. We can connect this result to the rate of the current increase at a given time, R, which can be represented as $R = \frac{\Delta I_{set}}{\Delta \tau}$. Since τ increases linearly with I_{set}, R can be simply reduced to $R = \frac{\Delta I_{set}}{\Delta \tau} \cong \frac{I_{set}}{\tau}$. Thus, R is constant for the OFF state and all the IRSs when V_{stress} is constant. On the other hand, we observed that the current did not increase any more when it reached a specific current value of the ON state, even though V_{stress} was applied for a long time (see Figure S6, Supporting Information). This means that R is constant during the turn-on process until the device reaches the maximum current state beyond which R changes to zero.

Figure 5a shows that the slopes of the I_{set} versus τ graphs increased as the V_{stress} increased, which means that the R increased with V_{stress}. The current increase over time can be interpreted as a formation of new current paths. This indicates that the current path formation rate was faster for larger V_{stress} since I_{set} increased rapidly with τ for large values of V_{stress}. Figure 5b shows the same data as Figure 5a but it displays a direct dependence of τ on V_{stress}. When V_{stress} linearly increased, τ exponentially decreased. This means that the current path formation rate exponentially depends on V_{stress} (see the inset of Figure 5b).

There are theoretical models which account for time–dependent dielectric breakdown that could be seen analogous to our observation.[29–32] Although we cannot specify which model

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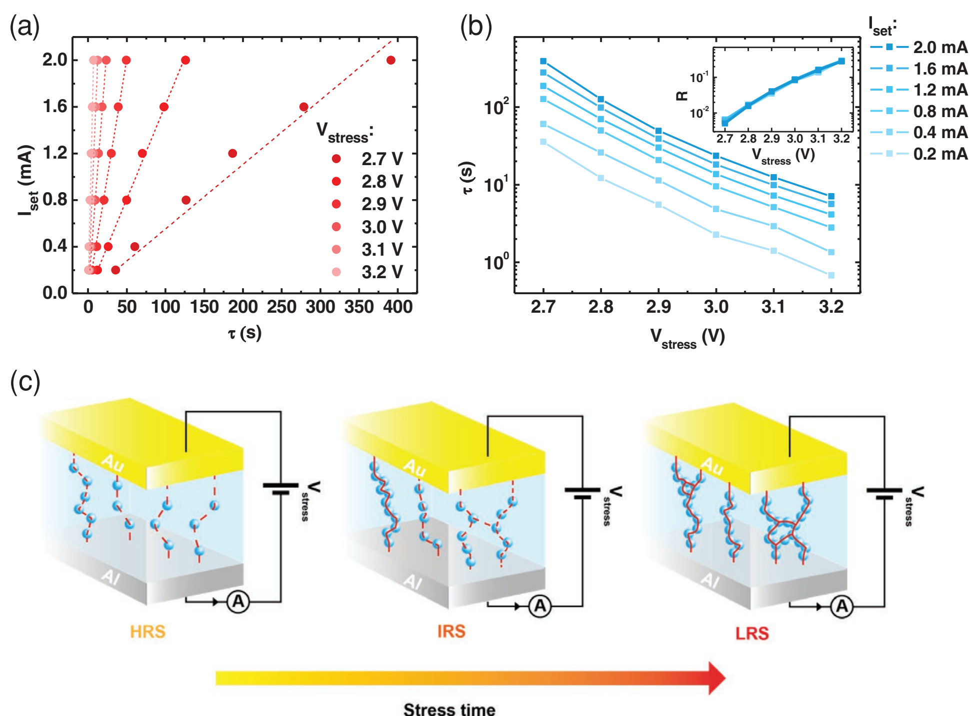

Figure 5. Dependence of the characteristic turn-on time, τ, on a) I_{set} under different V_{stress} and b) V_{stress} for different I_{set}. The calculated errors in τ are too small to be shown in the graph. The inset in (b) shows the dependence of the rate of current increase over time, R, on V_{stress}. c) A schematic representation of the overall turn-on process under a constant V_{stress} evolving from HRS (left) to LRS (right).

fully matches our data due to the limited range of V_{stress}, the common feature of the existing models (e.g., $\tau \propto \exp(-\sqrt{E})$,[27] $\tau \propto \exp(1/E)$,[29] and $\tau \propto \exp(-E)$,[33] where E is the electric field) is that they are all based on the electric breakdown via percolation current paths.

On the other hand, the exponential dependence of τ on E is highly relevant for the memory device operation, especially in writing and reading processes via voltage pulse operation. Our results predict that τ is 5.49×10^{10} s for V_{stress} of 0.3 V which is a reading voltage used for the device. During the reading operation of the OFF state, the probability of turn-on is 1.02×10^{-9}% for a reading voltage pulse of 0.3 V with a pulse-width of 1 ms. This is why the memory devices are highly unlikely to turn on during the reading operation at 0.3 V. On the other hand, τ is predicted to be 1.91×10^{-4} s for V_{stress} of 4.5 V. The probability of turn-on is 99.8% for a voltage pulse of 4.5 V with a pulse-width of 0.5 ms (see Section 7 in the Supporting Information for more details). Unfortunately, these values cannot represent all the PS:PCBM memory devices since the τ value is different for each device. In the worst case, the τ value is different by 2 orders of magnitude among the devices (see Figure S8, Supporting Information). Even after considering the device variation, the results from this work confirm the conclusion from our previous study which demonstrated that voltage pulses of the magnitude 4.5 V and the widths from 5 to 30 ms were sufficient to turn on the memory devices.[23] Therefore, our discovery of the probabilistic nature of the turn-on process enables us to provide guidelines on developing suitable pulse-operation protocols. This allows us to gain a greater control of the device operation by predicting the turn-on probability of the memory devices for various applied voltages and pulse-time-widths, which, in turn, can even be used to justify the previously reported 'trial-and-error' method of operating the devices.

Throughout the discussion, we have not identified the microscopic nature of the percolated conducting paths in the PS:PCBM memory device. Although we cannot provide a complete information on the composition, we have conducted further experiments to investigate the temperature–dependent charge transport and the environmental effect on the switching process in order to exclude some of the possible candidates (see Section 9 in the Supporting Information for details). Our analysis suggests that the conducting paths are composed of carbon-rich regions formed by pyrolysis between which tunneling-based conduction occurs.

Now, we suggest an overall picture of the turn-on process. During the SET process, a trap-limited conduction occurs in the highly resistive HRS (see 'HRS' in Figure 5c) which begins to initiate the formation of carbon-rich regions via Joule heating–induced pyrolysis. As a result, some of the carbon-rich regions become strongly connected which forms a current path in which the tunneling transport occurs, whereas other current paths remain weakly connected. This results in a slightly lower overall resistance and the current in the device is dominated by the well-connected current paths. The device becomes fully ON (i.e., LRS) when more carbon-rich areas are generated to form a larger number of strongly connected current paths ('LRS' in Figure 5c).

In order to check whether the probabilistic nature of the resistive switching process is universal for other active

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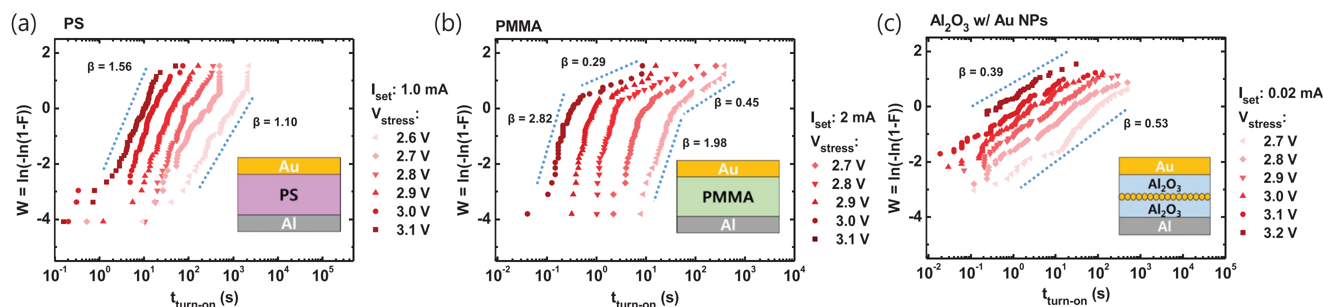

Figure 6. A linear fitting for the Weibull plots of $t_{\text{turn-on}}$ with the memory devices made of three other materials: a) PS, b) PMMA, and c) Al_2O_3 with Au NPs.

materials, we conducted the same tests on three different materials: PS, poly(methyl methacrylate) (PMMA), and Al_2O_3 with Au nanoparticles (NPs). The memory devices with the different active materials also turned on under a constant V_{stress} below the threshold voltage, showing similar behaviors of the stepwise current increase (see Figures S12–S14, Supporting Information). The measured $t_{\text{turn-on}}$ values of the memory devices made of all the different active materials could also be described by the Weibull distribution, as shown in **Figure 6**. The exponential dependence of τ and R with V_{stress} was also consistently observed for the different materials of PS, PMMA, and Al_2O_3 with Au NPs (see Figure S15, Supporting Information), which supports the percolated network model, like in PS:PCBM. Therefore, our results show that the different materials all show a probabilistic formation of percolated conducting paths. The observation implies the underlying common resistive switching properties in the different materials with different materialistic properties (i.e., varying from organic insulators, organic nanocomposites to inorganic insulators), as expected from the similar I–V curves of the memory devices (see Figures S12–S14, Supporting Information).

However, our results also reveal subtle differences between the resistive switching in the different material systems. The shape parameter, β, was found to be different for different materials which reflect different shapes of the percolation network of the conducting paths. For example, the correlation of β to the properties of the percolation network is seen clearly in the case of PMMA (Figure 6b), which shows degradation after the 11th cycle. After the degradation, the OFF current increases by an order of magnitude which may be due to the remaining strongly connected current paths. Concurrently, β increases sharply by an order of magnitude which indicates the formation of more localized conducting paths around these remaining strongly connected current paths, after the degradation. Although the change in β with respect to V_{stress} was similar for the devices with PS and PMMA cases, in the case of Al_2O_3 with Au NPs, the dependence of β on V_{stress} was not clear. A similar independency of β on V_{stress} has been previously reported for time–dependent dielectric breakdown measurements of inorganic gate dielectric materials for field-effect transistors.[18,34]

Our results demonstrate that both the experimental and statistical analysis techniques used for investigating time–dependent resistive switching behaviors can be applied to various material systems. This, combined with further experiments to identify the microscopic origin of the conducting paths, will be a powerful tool for understanding the resistive switching mechanism in memory devices.

3. Conclusion

We investigated the time–dependent turn-on phenomena of unipolar resistive memory devices by performing voltage-stress measurements. The turn-on time was observed to have a finite distribution which reflects an intrinsic probabilistic nature of the turn-on process. By statistically analyzing the turn-on time distribution, we found that the current paths formed a percolation network with shape properties and formation rate, both of which vary significantly with the stress voltage. Our results could be applied to estimate the turn-on probability of the memory devices during writing and reading processes via the pulse operation, which strengthens the practical relevance of this study for developing suitable operation protocols for unipolar resistive memory devices. We discovered that the probabilistic nature of the percolated conducting paths formation was shared between unipolar resistive memory devices with different active materials (PS, PMMA, and Al_2O_3 with Au NPs). Our results indicate that controlling these percolation current paths could enhance the electrical stability of the memory devices, which would be a key element for making practical memory devices. The analysis based on the Weibull statistics presented in this study may also be applicable for investigating the resistive switching properties of various other types of resistive memories.

4. Experimental Section

Device Fabrication: Al bottom electrodes with line-widths of 100 µm and a thickness of 30 nm were deposited by thermal evaporation through a shadow mask on cleaned SiO_2/Si substrates. UV-ozone was illuminated to clean the substrate and enhance the film quality of spin-coated PS:PCBM. Four different materials were used as the active layer—PS:PCBM, PS, PMMA, and Al_2O_3 with Au NPs. PS:PCBM and PS were made from solution mixtures of 32 mg of PS and 2.5 mg of PCBM dissolved in 4 mL of chlorobenzene and 8 mg of PS dissolved in 1 mL of chlorobenzene, respectively. The solutions were spin coated onto the bottom electrodes in ambient conditions and at a rate of 2000 rpm for 40 s. Then, the samples were soft-baked at 60 °C for 10 min. The contact pads of the bottom electrodes were exposed by an acetone-soaked Q-tip cotton swab. The samples were hard-baked at 120 °C for 60 min.

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The PMMA layers were made from a solution of 1% of PMMA with the molecular weight of 950 000 dissolved in anisole. The solution was spin coated onto the bottom electrodes at the rate of 4000 rpm for 40 s. After the exposure of the contact pads for contact with the swab, the samples were baked at 120 °C for 1 min. In case of the stacked layers of Al_2O_3/Au NPs/Al_2O_3, the three layers were sequentially deposited through the same shadow mask by an electron beam evaporator. The thicknesses of the active layers were ≈40 nm for PS:PCBM, ≈40 nm for PS, ≈40 nm for PMMA, and 20 nm/2 nm/20 nm for Al_2O_3/Au NPs/Al_2O_3 layers. The top gold electrodes with line-widths of 100 µm and a thickness of 30 nm were deposited through a shadow mask by electron beam evaporation for all the devices. The memory cell size was defined as 100 µm × 100 µm.

Device characterization: All the electrical measurements were performed in a vacuum environment (≈10^{-3} Torr) with a semiconductor parameter analyzer (Keithley 4200 SCS). The scan rate of the voltage sweep in *I–V* measurements was typically 0.54 V s^{-1}. The bias voltage was applied to Au top electrode while the Al bottom electrode was grounded. One cycle of the measurement was defined as a set of the current-stress-time scans from 2.7 to 3.2 V (i.e., 2.7 V stress, RESET, 2.8 V stress, RESET, ..., 3.2 V stress, and then RESET). In overall, 100 cycles of the voltage stress measurement were conducted for the PS:PCBM devices. The purpose of the measurement sequence was to reduce the systematic errors related to the voltage stress effect (e.g., device degradation).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

organic memory devices, time–dependent resistive switching, unipolar resistive memory devices, Weibull distribution

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