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Letter

Analysis of noise generation and electric conduction at grain boundaries in CVD-grown MoS_2 field effect transistors

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Abstract

Grain boundaries in a chemical vapour deposition (CVD)-grown monolayer of MoS_2 induce significant effects on the electrical and low frequency noise characteristics of the MoS_2. Here, we investigated the electrical properties and noise characteristics of MoS_2 field effect transistors (FETs) made with CVD-grown monolayer MoS_2. The electrical and noise characteristics of MoS_2 FETs were analysed and compared for the MoS_2 channel layers with and without grain boundaries. The grain boundary in the CVD-grown MoS_2 FETs can be the dominant noise source, and dependence of the extracted Hooge parameters on the gate voltage indicated the domination of the correlated number-mobility fluctuation at the grain boundaries. The percolative noise characteristics of the single grain regions of MoS_2 were concealed by the noise generated at the grain boundary. This study can enhance understanding of the electrical transport hindrance and significant noise generation by trapped charges at grain boundaries of the CVD-grown MoS_2 devices.

Supplementary material for this article is available online

Keywords: transition metal dichlcogendies, molybdenum disulphide, chemical vapour deposition, grain boundary, electrical noise, percolation behaviour

(Some figures may appear in colour only in the online journal)

1. Introduction

Molybdenum disulfide (MoS_2), a two-dimensional transition metal dichalcogenide (TMDC), has attracted remarkable attention as a promising semiconductor of next-generation nanoelectronics due to its unique electrical and mechanical properties [1–6]. MoS_2 and other TMDCs are typically prepared by a mechanical exfoliation method in a similar manner to which an atomic film of graphene was first prepared [7–10]. However, to utilize MoS_2 in large-area integrated applications, it is desirable to grow uniform large-area MoS_2 using techniques such as the chemical vapour deposition (CVD) synthesis method [11–17]. When MoS_2 films are grown using CVD, it is well-known that the electrical performance of CVD-grown MoS_2 is limited by structural defects which are created during the synthesis process [18–22]. Grain boundaries in CVD-grown MoS_2 can be trap sites which must be avoided for low-signal sensors or AC operating applications, as the dimension of MoS_2 devices is scaled down to the sub-μm regime [22]. The effects of grain

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boundaries on the electrical performance and noise characteristics in CVD-grown MoS_2 require a thorough understanding to increase their potential for future applications. In this regard, the electrical analysis with low frequency $1/f$ noise characterization can be an effective approach by providing insights into the determination of the dominant noise source between carrier mobility fluctuation and carrier number fluctuation, as well as the information of conductive paths in the channel layer [22–27]. Recently, Hsieh *et al* reported that carrier localization length can be significantly reduced at grain boundaries of CVD-grown MoS_2 films from the temperature dependence of the electric transport properties [22]. The strongly localized electronic channel within the grain boundary was reconfirmed by the enhanced low-frequency noise by one to three orders of magnitude [22]. However, the exact noise generation mechanism from the grain boundaries needs to still be addressed.

In this work, we investigated the effect of grain boundaries in CVD-grown monolayer MoS_2 on the electrical characteristics using electrical noise measurements. The electrical and noise characteristics of MoS_2 FETs with and without grain boundaries were analysed and compared. In particular, the relation between the Hooge parameters and gate bias indicated the domination of correlated number-mobility fluctuation at the grain boundaries. A low exponent value in the power-law relation between relative noise and resistance indicated that the noise in MoS_2 with grain boundaries is primarily generated from grain boundary regions. These results support that grain boundaries are the dominant noise source by acting as trap sites, which affect the current fluctuation in CVD-grown MoS_2 FETs.

2. Experimental details

2.1. Growth of monolayer MoS_2 and device fabrication

The uniform monolayer MoS_2 was grown on a SiO_2/Si substrate using a CVD system (Teraleader Co., Korea). The substrate had a 270 nm thick SiO_2 layer on heavily doped p++ Si. Boats with MoO_3 and sulfur powder were placed in the middle and upper position of the tube in the CVD system, respectively. The detailed CVD growth process of monolayer MoS_2 has previously been reported [12]. Figure 1(a) explains the fabrication process of MoS_2 FETs. To prevent the potential leakage of current through the SiO_2 layer, which might have been damaged during the CVD process, the CVD-grown MoS_2 films were transferred to the other SiO_2/Si substrate using the poly(methyl methacrylate) (PMMA)-assisted transfer method [16]. A thermal tape was attached as a supporting layer, and entire parts (thermal tape, PMMA, MoS_2, SiO_2, and Si) were submerged in a potassium hydroxide solution (~25%) to separate the MoS_2 films from the SiO_2/Si substrate. After the separated MoS_2 film is attached to the other SiO_2/Si substrate, an isolated and large MoS_2 piece (~10 μm size) with grain boundaries was selected to make the MoS_2 FETs with and without grain boundaries. Next, a pattern was designed for the source and drain electrodes by an e-beam lithography system (JSM-6510, JEOL). Finally, Au (50 nm)/Ti (5 nm) layers were deposited by an e-beam evaporator (KVE-2004L, Korea Vacuum Tech.) at a pressure of $\sim 10^{-7}$ Torr to form the source and drain electrodes. The electrical performance of TMDC FETs has been limited by contact resistance. In this regard, the contact resistance of the CVD-grown MoS_2 FET was extracted by Y-function method. The extracted value of contact resistance was 68.02 kΩ and comparable to the reported value of previous studies (see figure S1 and table S1 in supplementary data available online at stacks.iop.org/NANO/28/47LT01/mmedia). This result indicates that the contact resistance between MoS_2 channel and metal contacts did not deteriorate significantly the electrical characteristics of the CVD-grown MoS_2 in this work.

When monolayer MoS_2 films are grown by CVD, single grains of MoS_2 are formed as a triangular shape and grain boundaries exist between the merged MoS_2 triangles [11, 17–22]. Therefore, we could fabricate both MoS_2 FETs with and without grain boundaries from a large enough piece of MoS_2 film. Figure 1(b) shows the optical image of fabricated both MoS_2 FETs with and without grain boundaries from a MoS_2 flake. In this figure, the grain boundaries are indicated by white dashed lines in a MoS_2 flake that is indicated by a black dashed line, and some MoS_2 FET devices include a grain boundary, while others do not.

2.2. Raman and photoluminescence (PL) characteristics of CVD-grown monolayer MoS_2

To confirm the number of layers of the CVD-grown MoS_2, Raman and PL spectra were measured (figure 1(c)). An A1 peak (~1.85 eV) was observed in the PL spectra. The two peaks, which represent the in-plane E^1_{2g} and the out-of-plane A_{1g} vibration, were shown in the Raman spectra (the inset of figure 1(c)). The difference between two peaks of Raman spectra was 20.09 cm^{-1}. The peak values in PL and Raman spectra are similar to the known values of monolayer of MoS_2 [28–30], which supports that our CVD-grown MoS_2 films are indeed a monolayer.

2.3. Current–voltage (I–V) characteristics

The electrical characteristics of the CVD-grown MoS_2 FET devices were measured using a semiconductor parameter analyser (Keithley 4200, USA) in the dark and under a vacuum (~10^{-3} Torr). Before measurement, the CVD-grown MoS_2 devices were heated at 400 K under a vacuum for about six hours to eliminate adsorbates from the MoS_2 surface, such as water, oxygen molecules, and polymer residue [20]. These adsorbates can work as trap states, which induce electrical noise in the MoS_2 FETs. To scrutinize the effect of the grain boundary on the noise characteristics of the CVD-grown MoS_2 FET, this annealing process can reduce other noise sources from the interface interaction.

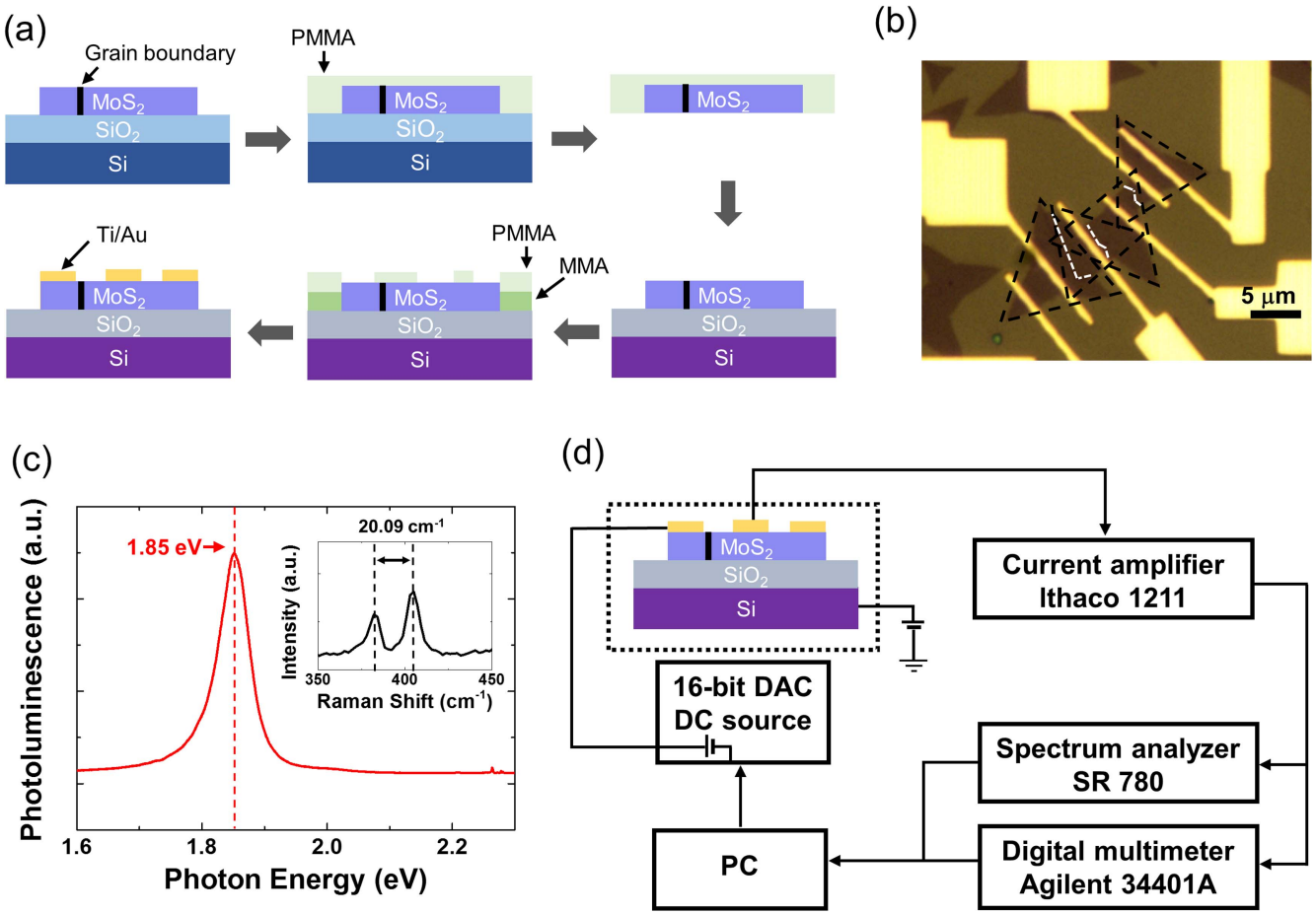

Figure 1. (a) Schematic illustration of the fabrication processes for CVD-grown MoS_2 FETs with and without grain boundary. (b) Optical image showing CVD-grown MoS_2 FETs with and without grain boundary made from a MoS_2 flake. (c) Raman and PL spectra of CVD-grown monolayer MoS_2. (d) Schematic of the noise measurement setup.

2.4. Electrical noise characteristics

Figure 1(d) shows a schematic of the noise measurement setup. A 16 bit digital-analogue converter was used to apply the voltage bias. A battery-powered current amplifier (Ithaco 1221) was used for amplifying the current fluctuation. A spectral analyser (SR760) and a digital multimetre (Agilent 34401A) were used to monitor the frequency domain noise signal (power spectral density) and obtain the average electrical current, respectively. Current fluctuations between the source and drain electrodes were measured, while a back-gate bias was applied.

3. Results and discussion

Since the geometries of MoS_2 FETs with and without grain boundaries are different from each other, the current level from the characteristic curve was normalized to the channel width (W) and length (L) to compare the electrical conductions. The normalized current, I_{norm}, was defined as $I_{norm} = I_{DS} \times L/W$, where I_{DS} is the source-drain current. The transfer characteristics, i.e., normalized current versus source-gate bias (I_{norm}–V_{GS}), of both MoS_2 FETs with and without grain boundaries exhibited a typical n-type semiconductor behaviour (figures 2(a) and (b)). The output characteristics (I_{DS}–V_{DS}) of both MoS_2 FETs are also shown in the inset of figures 2(a) and (b). As shown in these figures, the current level of the MoS_2 FET without a grain boundary was higher than that of the MoS_2 FET with a grain boundary. To more explicitly compare the current level between the two MoS_2 devices with and without a grain boundary, the ratio of I_{norm}^{GB} to I_{norm}^{SG} was calculated with V_{GS} varying from 10 to 40 V with a step of 10 V and V_{DS} varying from 0.5 to 2.0 V with a step of 0.5 V, where SG and GB denote the sample with a single grain without a grain boundary and the sample with a grain boundary, respectively (figure 2(c)). The ratio values were found to be less than 0.2, which means the current of MoS_2 FET without a grain boundary is about five times higher than that of MoS_2 FET with a grain boundary.

To further investigate the effect of a grain boundary on the electrical characteristics of MoS_2 FETs, mobility values of three sets of MoS_2 FETs with and without a grain boundary were extracted from the electrical characterization and compared (figure 2(d)). As shown in this figure, the mobility values of the MoS_2 FETs with a grain boundary were two to four times lower than those of the devices without a grain boundary. This substantial reduction in the mobility of the MoS_2 FETs with a grain boundary implies that the charge

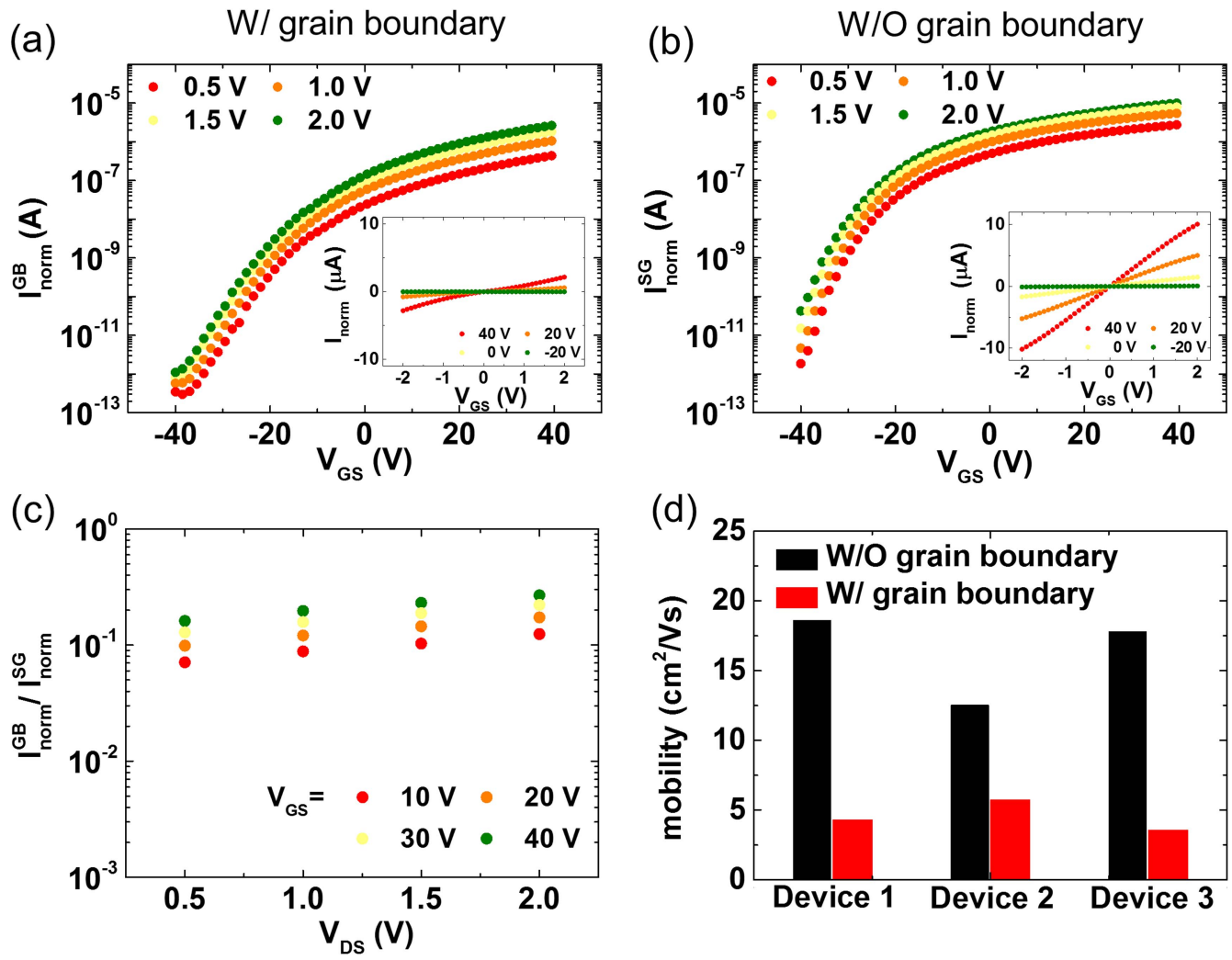

Figure 2. I_{DS}–V_{GS} curves of CVD-grown MoS_2 FETs (a) with and (b) without grain boundary for different drain bias. The insets indicate the I_{DS}–V_{DS} curves of the same device for different gate bias. (c) The ratio of I^{GB}_{norm} to I^{SG}_{norm} for different gate and drain bias. (d) A histogram showing the mobility values of three sets of CVD-grown MoS_2 FETs with and without grain boundary.

carriers at the grain boundary undergo a significant hindrance in the electrical transport. This hindering effect of the grain boundary can be attributed to trap states formed at the grain boundary, which can be electrical noise sources. The restriction of charge transport at the grain boundary in CVD-grown MoS_2 has also been observed in previous studies [21, 22]. Furthermore, the mobility of the CVD-grown MoS_2 was not significantly affected by the misorientation angle (>20°) between two coalescing grains, which is consistent with previous studies (see table S2 in the supplementary data) [21].

To investigate the effect of a grain boundary on the electrical noise of the CVD-grown MoS_2 FETs, low frequency noise characteristics of the MoS_2 FETs with and without a grain boundary were measured and compared. The relative power spectral densities of current signals (S_I/I^2) of both MoS_2 FET devices with and without a grain boundary measured at a fixed $V_{DS} = 2$ V and V_{GS} ranging from 40 to −10 V show a $1/f$ type noise at low frequency (up to 10 000 Hz) (figures 3(a) and (b)). The noise spectral density of the CVD-grown MoS_2 was almost independent of misorientation angle between coalescing grains (see table S2 in the supplementary data) [22]. The relative noise levels and gate bias dependence of the device without a grain boundary were similar to previous study [20]. However, the relative noise levels of the device with a grain boundary had less variation by the gate biases compared to the device without a grain boundary.

Figure 3(c) shows the relative noise of the MoS_2 FETs with and without a grain boundary at $V_G = 40$ V. The grain boundaries in the CVD-grown MoS_2 films increase the relative noise of the MoS_2 FET more than ten times. For a more correct comparison of the noise levels, an area normalization of the relative noise should be considered. In most transistor devices, the reversely proportional relation between the relative noise amplitude and device area ($f \cdot S_I/I^2 \propto (WL)^{-1}$) has been observed with several models, such as the Hooge's empirical relation, the interfacial trapping model, and the variation-range-hopping fluctuation model [31, 32]. Therefore, the relative noise, normalized to the device area, was

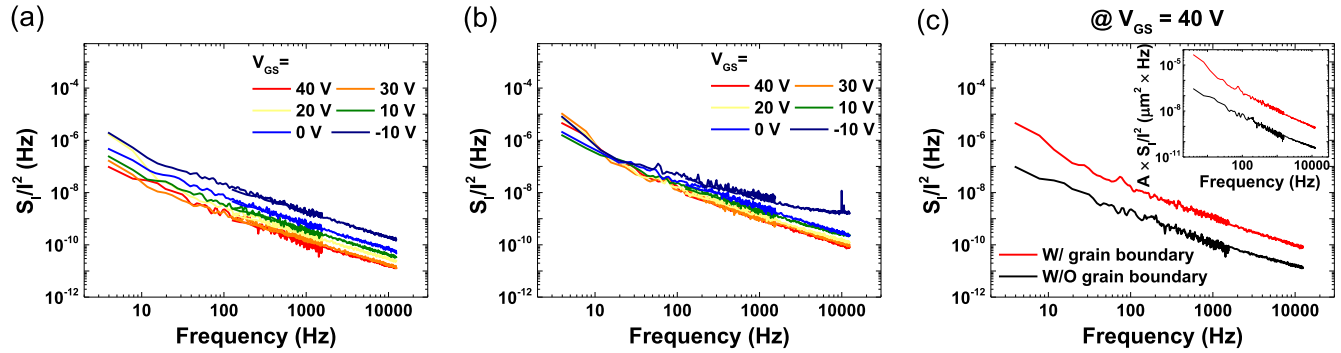

Figure 3. The relative noise of CVD-grown MoS_2 FETs (a) with and (b) without grain boundary for different gate bias. (c) The relative noise of CVD-grown MoS_2 with and without grain boundary at a fixed $V_{GS} = 40$ V. The inset indicates the relative noise normalized to device area.

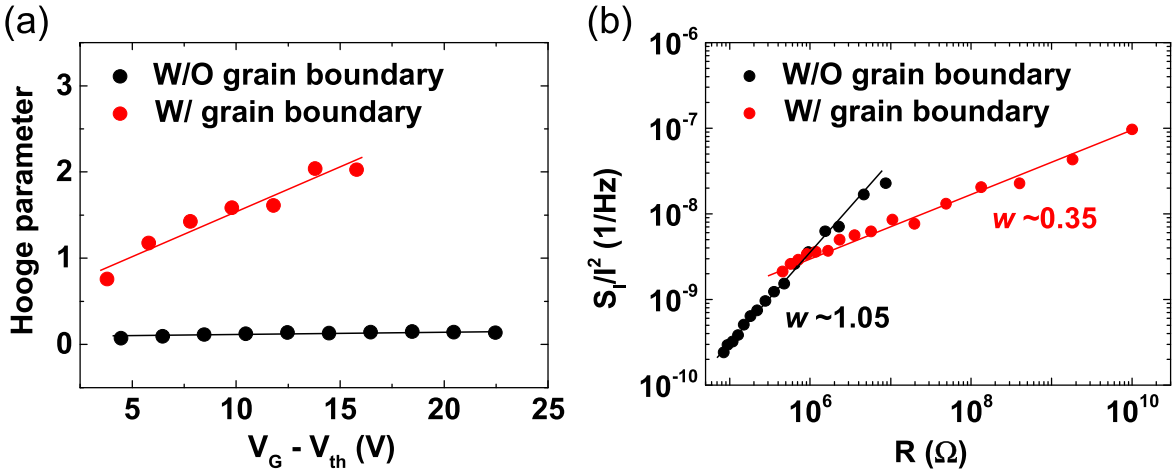

Figure 4. (a) The Hooge parameters of CVD-grown MoS_2 FETs with and without grain boundary for different $V_{GS} - V_{th}$. (b) Power-law relation between the relative noise and resistance of CVD-grown MoS_2 FETs with and without grain boundary.

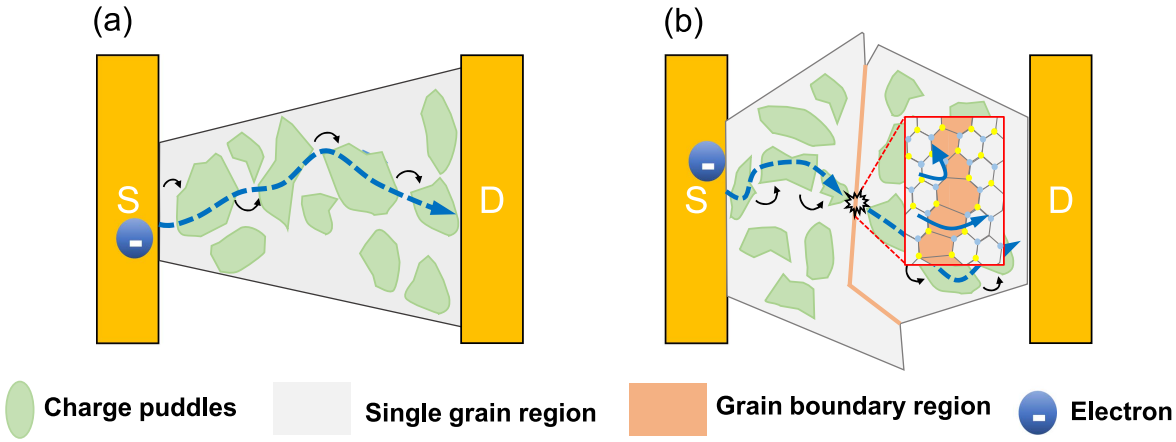

Figure 5. Schematic illustration of carrier conduction in CVD-grown MoS_2 FETs (a) with and (b) without grain boundary.

defined as $A \times S_I/I^2$, where A is the device area. $A \times S_I/I^2$ of the MoS_2 FETs with and without a grain boundary is shown in the inset of figure 3(c). As shown in the inset of figure 3(c), $A \times S_I/I^2$ of MoS_2 FET with a grain boundary was still more than ten times higher than that of MoS_2 FET without a grain boundary. These results indicate that grain boundaries can be regarded as a dominant noise source in the CVD-grown MoS_2 films. The $1/f$ type noise in transistor devices has been explained by several sources of charge carrier fluctuations, such as Hooge mobility fluctuation, McWhorter carrier number fluctuation, and correlated number-mobility fluctuation [31–36]. Through analysing the gate bias dependence of current noise of the MoS_2 FETs with and without a grain boundary using these models, noise sources of

MoS_2 FETs with and without a grain boundary can be discriminated. The gate bias dependence of the Hooge parameter can be a useful guideline for determining the dominant noise source. In the case of mobility fluctuation, the Hooge parameter is independent of the total charge carrier number (N) [37–39]. On the other hand, the Hooge parameter is proportional to $1/N$ in case of McWhorter number fluctuation [36, 38, 40]. The Hooge parameter can be extracted using Hooge's empirical relation, which is expressed as

$$\frac{S_I}{I^2} = \frac{\alpha_H}{N}\frac{1}{f}, \tag{1}$$

where S_I is the current power spectral density, I is the current, α_H is the Hooge parameter, N is the total number of free charge, and f is the frequency [37–40]. In the case of FET devices, the total number of free charge N can be calculated as $N = (V_{GS} - V_{th})AC_i/q$ with the condition of a small V_{DS}, where V_{th} is the threshold voltage, A is the area of the device, C_i is the gate dielectric capacitance of the device, and the q is the elementary charge.

Using Hooge's empirical relation and N, the Hooge parameters of the MoS_2 FETs were extracted as the function of $V_{GS} - V_{th}$ (figure 4(a)). With the MoS_2 FET without a grain boundary, the Hooge parameters were nearly constant ($\sim$0.14) with $V_{GS} - V_{th}$, which can be explained by the mobility fluctuation model [38, 40]. Note that the gate dependence of the relative noise, consistent with the Hooge model, has been reported in mechanically exfoliated monolayer MoS_2 [41]. The linearly increasing behaviour of the Hooge parameters, with increasing $V_{GS} - V_{th}$, can be explained by the correlated number-mobility fluctuations model, where the carrier number fluctuation at traps influences the carrier mobility fluctuation [35]. In the correlated number-mobility fluctuations model, α_H becomes linearly proportional to N under the condition of a sufficiently small drain voltage and large N, which means $\alpha_H \sim (V_{GS} - V_{th})$. The Hooge parameter behaviour, explained by the correlated number-mobility fluctuation model, implies that trapped carriers at the grain boundary can be considered as scattering centres in CVD-grown MoS_2 films, and the number of trapped carriers at the grain boundary can fluctuate. The number fluctuation of trapped carriers can cause the fluctuation of scattering rate; when this occurs at the grain boundary, it can lead to the correlated carrier number-mobility fluctuation.

The CVD grown-MoS_2 can be considered to have a disordered electronic structure, which has randomly distributed charge puddles due to the large trap density originated from structural defects, such as sulfur vacancies, dielectric impurities, and grain boundaries [16]. A disordered conductive system can be regarded as a random resistor network [42]. Hopping of charge carriers between neighbouring charge puddles can be considered, as the current flows through randomly distributed resistors. According to percolation theory, the electrical characteristics of a random resistor network are determined by a conductive phase fraction p. Additionally, a conductive channel is formed when p exceeds the percolation threshold p_c. The relation between the electrical noise and resistance of a random network resistor system obeys the following power-law relation [42–44]

$$\frac{S_I}{I^2} = \frac{S_R}{R^2} = \frac{\sum_m \tilde{S}(f)_m\, i_m^4}{\left(\sum_m i_m^2\right)^2} \propto R^w \text{ at } p > p_c, \tag{2}$$

where S_I is the power spectral density for current signal, S_R is the power spectral density for resistance signal, i_m denotes the current flowing in mth resister, $\tilde{s}(f)_m$ is the spectral density of factional noise of mth resistor, and R is the total resistance of percolating network. Higher gate bias lowers the potential barrier between charge puddles, modulating the connection of the conductive network in the MoS_2 layer [45]. Therefore, various S_I/I^2 and R values were obtained by modulating the gate bias. Our CVD-grown MoS_2 FET devices exhibited the power-law behaviour between the relative noise and resistance, which can be considered as percolative behaviour (figure 4(b)). In the MoS_2 FET without a grain boundary, the power-law exponent w was found to be $\sim$1.05, which is a comparable value of w reported from previous noise study on single grain MoS_2 [20]. On the other hand, the w value of the MoS_2 FET with a grain boundary was found to be $\sim$0.35, which is much smaller than the exponent in the single grain MoS_2. This low value of w has not been expected from the available percolation theories, which could indicate that the percolation is not geometrical [46–48]. This non-geometric property can be attributed to the grain boundary, which has one-dimensional geometry. Therefore, the percolative noise characteristics from single grain MoS_2 regions were concealed by the larger noise generation from the grain boundary. In short, the large noise generation at the grain boundary by the correlated number-mobility fluctuation predominated over the noise generated from the resistor network of the single grain MoS_2.

Figures 5(a) and (b) illustrate the schematics of conductive network in the CVD-grown MoS_2 FETs without and with a grain boundary, respectively. In case of the MoS_2 FET without a grain boundary, the charge carriers in one of the charge puddles can hop to the neighbouring charge puddle, which can be regarded as the current flowing in one of the randomly distributed resistors. On the other hand, in case of the MoS_2 FET with a grain boundary, the charge carriers can hop to another charge puddle, similar to the carriers in MoS_2 FET without a grain boundary. However, charge carriers in MoS_2 FET with a grain boundary can be trapped at the grain boundary as energy levels near the Fermi level can be induced by the dislocations in the grain boundary [21]. These trapped carriers can play as scattering centres, undermining the electrical characteristics of the MoS_2 devices. Additionally, the scattering at the grain boundary can generate a considerable amount of noise, concealing the noise characteristics of the random resistor network in single grain MoS_2. Trapping/de-trapping events of charge carriers can induce fluctuation of the scattering rate at the grain boundary, which can be observed as the correlated number-mobility fluctuation.

4. Conclusion

The electrical and noise characteristics of CVD-grown monolayer MoS_2 FET devices with and without a grain boundary were investigated. The electrical transport in CVD-grown MoS_2 FETs were hampered by the grain boundary, which can be considered as the dominant noise source. According to the gate bias dependence of the Hooge parameters, the correlated number-mobility fluctuation at the grain boundary generates large noise in CVD-grown MoS_2 films. From the relation between the relative noise and resistance values, the noise generated at the grain boundary concealed the percolative noise characteristics of the single grain regions of MoS_2. This work provides insight into how a grain boundary hinders the electrical transport and can be a significant noise source of CVD-grown MoS_2 devices.

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