2D Materials

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Large scale MoS_2 nanosheet logic circuits integrated by photolithography on glass

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Abstract

We demonstrate 500 × 500 μm^2 large scale polygrain MoS_2 nanosheets and field effect transistor (FET) circuits integrated using those nanosheets, which are initially grown on SiO_2/p^+–Si by chemical vapor deposition but transferred onto glass substrate to be patterned by photolithography. In fact, large scale growth of two-dimensional MoS_2 and its conventional way of patterning for integrated devices have remained as one of the unresolved important issues. In the present study, we achieved maximum linear mobility of ~9 $cm^2\ V^{-1}\ s^{-1}$ from single-domain MoS_2 FET on SiO_2/p^+–Si substrate and 0.5~3.0 $cm^2\ V^{-1}\ s^{-1}$ from large scale MoS_2 sheet transferred onto glass. Such reduced mobility is attributed to the transfer process-induced wrinkles and crevices, domain boundaries, residue on MoS_2, and loss of the back gate-charging effects that might exist due to SiO_2/p^+–Si substrate. Among 16 MoS_2-based FETs, 13 devices successfully work (yield was more than 80%) producing NOT, NOR, and NAND logic circuits. Inverter (NOT gate) shows quite a high voltage gain over 12 at a supply voltage of 5 V, also displaying 60 μs switching speed in kilohertz dynamics.

1. Introduction

After graphene [1, 2], two-dimensional (2D) nanosheet semiconductor materials with discrete bandgap have attracted much attention from many researchers owing to their interesting physical properties and potentials for future nanoscale electronics [3–7]. Like graphene, those 2D semiconductors are formed by mechanical exfoliation using scotch tapes in general. Among many nanosheet materials, molybdenum disulfide (MoS_2), a transition metal dichalcogenide (TMD) [8–10] semiconductor has been the most extensively studied, since it has displayed excellent carrier mobility, high on/off current ratio, and good subthreshold swing in a field-effect transistor (FET) form with n-type conduction [11–16]. However, fabricating 2D MoS_2 by the mechanical exfoliation limits the length scale only to a few micrometers. So, one of the remaining important issues is how to fabricate such 2D MoS_2 in a large scale, which would open the gate toward more practical applications enabling conventional photolithography for device/circuit patterning. Several research groups have thus recognized the issue, studying and reporting on the chemical vapor deposition (CVD) of large scale MoS_2 2D sheets [17–20]. Yet, only a few studies of full photolithographic patterning and integration for polygrain 2D MoS_2-based devices in large scale have been reported [21, 22], to the best of our limited knowledge.

In the present work, we demonstrate 500 × 500 μm^2 large scale polygrain MoS_2 nanosheets and FET logic circuits integrated using those nanosheets, which are initially grown on SiO_2/p^+–Si by CVD but transferred onto glass substrate to be patterned by photolithography. Maximum linear mobility of our single-domain MoS_2 FET ~9 $cm^2\ V^{-1}\ s^{-1}$ on SiO_2/p^+–Si substrate but appears reduced to be 0.5~3.0 $cm^2\ V^{-1}\ s^{-1}$ when MoS_2 sheet is transferred onto glass. It is due to the transfer process-induced wrinkles and crevices [23, 24], domain boundaries [25–28], residue on MoS_2 [29, 30], and loss of the back gate-charging effects [31–35] that might exist due to

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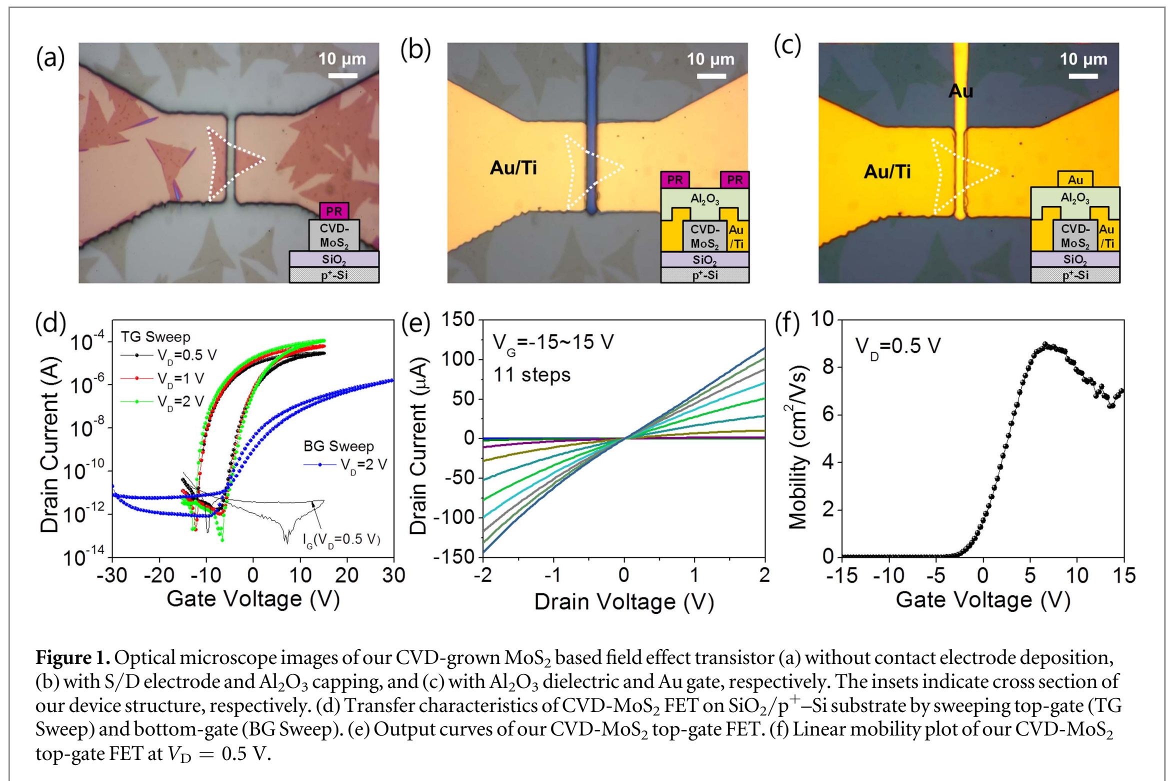

Figure 1. Optical microscope images of our CVD-grown MoS_2 based field effect transistor (a) without contact electrode deposition, (b) with S/D electrode and Al_2O_3 capping, and (c) with Al_2O_3 dielectric and Au gate, respectively. The insets indicate cross section of our device structure, respectively. (d) Transfer characteristics of CVD-MoS_2 FET on SiO_2/p^+–Si substrate by sweeping top-gate (TG Sweep) and bottom-gate (BG Sweep). (e) Output curves of our CVD-MoS_2 top-gate FET. (f) Linear mobility plot of our CVD-MoS_2 top-gate FET at $V_D = 0.5$ V.

SiO_2/p^+–Si substrate. Among 16 MoS_2-based FETs, 13 devices successfully work (yield was more than 80%) producing NOT, NOR, and NAND logic circuits. Inverter (NOT gate) shows quite a high voltage gain over 12 at a supply voltage of 5 V, also displaying 60 μs switching speed in kilohertz dynamics.

2. Results and discussion

Optical microscopy (OM) image of figure 1(a) displays CVD-grown MoS_2 flakes covering only partial area of the SiO_2/p^+–Si substrate, where a large triangular MoS_2 flake now appears ready for source/drain (S/D) electrode patterning with photoresist (PR) (inset cross section) on. One side of the single triangular MoS_2 flake was longer than 15 μm and the flake thickness was reported to be ~1 nm at the most edge but should not be uniform particularly at the center of triangle since it has gone through nucleation and growth processes starting from central nucleus or seed [17, 36]. Figure 1(b) shows the top view of FET with S/D electrode and Al_2O_3 capping layer, on which PR-pattern was now ready for gate definition (see inset cross section as bottom gate MoS_2 FET form), while figure 1(c) exhibits a finalized form of top-gate patterned FET with Al_2O_3 dielectric and Au gate. Figure 1(d) displays the drain current–gate voltage (I_D–V_{GS}) transfer curves of top- and bottom-gate FETs, respectively while figure 1(e) shows drain current–drain voltage (I_D–V_{DS}) output behavior of top-gate FET which appears very ohmic. Maximum linear mobility (μ_{Max}) is estimated to be ~9 $cm^2\,V^{-1}\,s^{-1}$ as shown in the plot of figure 1(f). Such mobility value is regarded quite comparable to previous reports [36].

In our study, the transfer of CVD-grown MoS_2 flake/or film was attempted, so that we might fabricate the FETs and integrated circuits on glass in large scale. Figure 2(a) shows the basics of transfer processes, according to which polymeric PMMA spin coating to attach MoS_2 flake is initially implemented and then the solid PMMA with flake can be free by removing SiO_2 film (by KOH solution treatment) [37, 38]. The PMMA-attached MoS_2 is then transferred onto the glass substrate, to be a channel of top-gate FET as respectively shown in figure 2(b) and its inset for top- and bottom-illumination OM images, (gate electrode was indium–tin–oxide (ITO)). The linear mobility of the glass-substrate MoS_2 FET appears limited to only ~0.9 $cm^2\,V^{-1}\,s^{-1}$ (according to figure 2(c) and its inset plot) which is an order of magnitude lower than that of SiO_2/p^+–Si-supported MoS_2. Positive part is that the gate sweep-induced hysteresis becomes as small as 0.6 V on glass while that on SiO_2/p^+–Si was as large as ~4 V. We attribute the small hysteresis to the fact that glass substrate does not charge the back channel of top-gate MoS_2 FET while SiO_2/p^+–Si substrate may charge the back (bottom) channel somewhat activating bottom interface as well. But no back gate-charging [31–35] makes I_D and apparent mobility smaller on glass, either. Besides, transfer-induced wrinkles and chemical (PMMA/KOH)-residue on MoS_2 surface influence the mobility in very negative ways [29, 30]. Similar effects have been reported comparing the devices fabricated on SiO_2/p^+–Si and glass substrates [39].

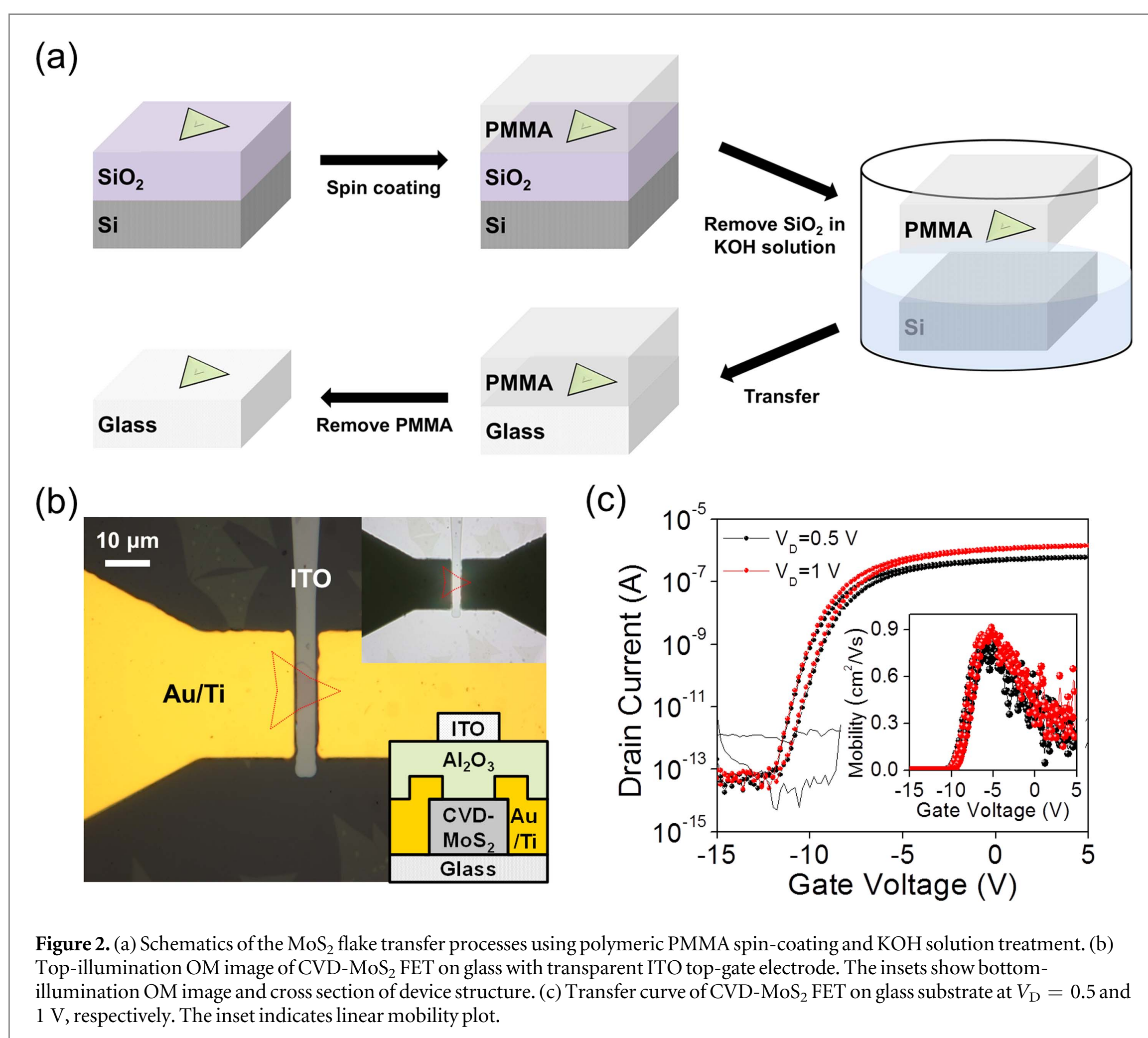

Figure 2. (a) Schematics of the MoS_2 flake transfer processes using polymeric PMMA spin-coating and KOH solution treatment. (b) Top-illumination OM image of CVD-MoS_2 FET on glass with transparent ITO top-gate electrode. The insets show bottom-illumination OM image and cross section of device structure. (c) Transfer curve of CVD-MoS_2 FET on glass substrate at $V_D = 0.5$ and 1 V, respectively. The inset indicates linear mobility plot.

Based on above results of figures 1 and 2, we attempted to cover a 500 μm × 500 μm large area of glass substrate by CVD MoS_2 growth and flake transfer. Figure 3(a) displays such a large area of MoS_2 grown on SiO_2/p^+–Si substrate observed under OM while figure 3(b) does show the same image observed after film transfer onto glass. Triangular flakes grow and are merged to make a large area, but monolayer thickness might be maintained except the small seed areas of large grains (according to Raman spectroscopy results of figure S1, the seed area turns out to have bilayer-thickness). The area coverage was ~99% in fact, almost covering whole 500 μm × 500 μm area. Figures 3(c) and (d) respectively show the PR-selected and O_2 plasma etch-patterned MoS_2 areas for FET channels (16 in total). Figures 3(e) and (f) display 16 sets of patterned Au/Ti S/D and gates, respectively. After 50 nm-thick Al_2O_3 deposition by ALD, we patterned two types of top gate metal with ITO and Au/Ti on Al_2O_3 to distinguish FETs by optical contrast. Red-dotted area indicates MoS_2 channels covered by S/D, Al_2O_3 top dielectric, and gate metal. We prepared another set of FET arrays with slightly different gate pattern, which was examined by scanning electron microscopy (SEM) in figure 3(g) and a red-dotted area (gate region) was magnified in figure 3(h), where many of MoS_2 domain boundaries are observed and indicated by white-dotted lines as an evidence of merged MoS_2 flakes. Lastly, AFM images of C1, C2, and C3 area in figure 3(d) (for MoS_2 channels on glass) are shown in figure 3(i). According to atomic force microscope (AFM) images of figure 3(i), uncovered or crevice areas appear dark and wrinkles look white as probably formed during flake transfer, and central small triangles as MoS_2 seed nuclei are also observed. It is regarded that such wrinkles, crevices (figure 3(i)), and domain boundaries (figure 3(h)) should play as carrier scattering centers together with the chemical residue on MoS_2 surface, decreasing the mobility of FET. Interestingly, little wrinkles and crevices are observed from initial large scale MoS_2 layer on SiO_2/p^+–Si substrate as seen in AFM results of figure S2. So, one would expect better mobility results from any large scale patterned MoS_2 FETs on SiO_2/p^+–Si substrate. However, in fact, our CVD-grown MoS_2 on SiO_2/p^+–Si basically showed inferior adhesion which was not sufficient enough to go through photolithography processes in large scale, while its adhesion on glass becomes strong enough after the layer transfer.

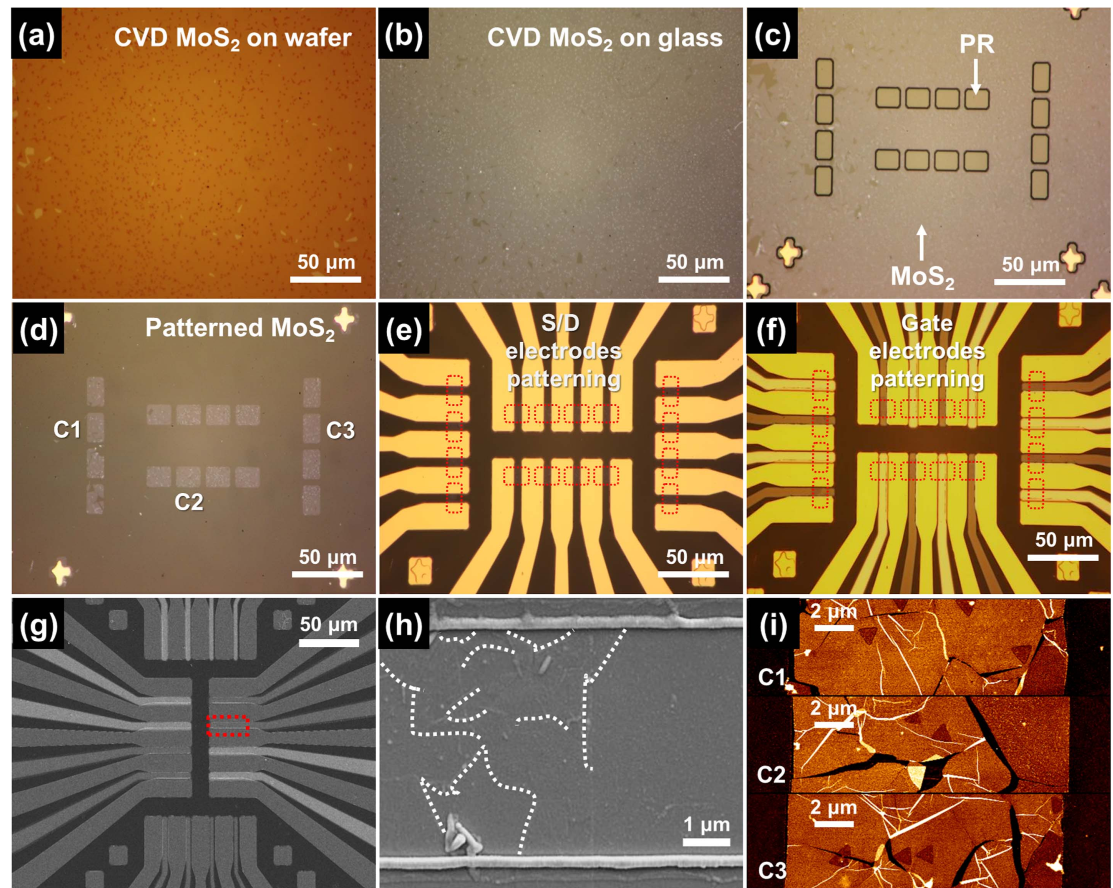

Figure 3. Optical microscope images of large area MoS_2. (a) As-grown state on SiO_2/p^+–Si substrate, (b) transferred on glass substrate, (c) PR-selected, (d) patterned MoS_2 area for 16 FET channels by O_2 plasma etching, (e) patterned Au/Ti source/drain electrode, and (f) patterned opaque Au/Ti and transparent ITO top-gate electrode, respectively. SEM images (g) of our 16 CVD-MoS_2 FETs and (h) from the corresponding red-dotted area in (g) while white-dotted lines indicate MoS_2 domain boundaries. (i) AFM images of patterned MoS_2 channels in C1, C2, C3 area of figure 3(d).

Figures 4(a) and (b) display the transfer curve characteristics (drain current–gate voltage: I_D–V_{GS}) of five Au/Ti- and eight ITO-top gate FETs. Output (I_D–V_{DS}) and gate leakage (I_G–V_{GS}) characteristics are shown in figure S3. Among total 16 FETs, 13 devices are operating and their threshold voltages (V_{Th}s) were in a range between −1 and −4 V as shown in the plot in figure 4(c). Three FETs with Au/Ti gate among 16 devices did not properly operate showing too small I_D current (see figure S4), probably because the patterned channel area incidentally contains too many of MoS_2-crevice region (e.g. case C2 and C3 in figure 3(i)). Linear mobility of our FETs with Au/Ti and ITO gates are respectively plotted in the insets of figures 4(a) and (b), where the mobility appears scattered in range between 0.5 and ~3 $cm^2 V^{-1} s^{-1}$ (also see figure 4(c) for summary). Figure 4(d) shows a photograph for our 16 FET arrays with S/D and G electrode pads on glass.

Selecting two neighbored (but electrically isolated) FETs with different transfer curves (or mobility) of figures 5(a) and (b), a logic inverter (NOT gate) was formed as shown in an OM image and overlaid circuit of figure 5(c). Here, Au/Ti-gated FET with smaller I_D plays as a driver while ITO gated FET does as a load. The load FET appears to show ~7 times higher I_D than that of driver FET according to the inset output characteristics in figures 5(a) and (b). As a result, we obtained voltage transfer characteristics (VTC) of figure 5(d) changing supply voltage (V_{DD}) from 2 to 10 V. Maximum voltage gain appears to be ~16 at 10 V of V_{DD} (~12 at 5 V V_{DD}) while transition voltage was ~5 V. Dynamic inverter switching behavior is well demonstrated at 100 and 1000 Hz under 2 V V_{DD} in figures 5(e) and (f), respectively, and 60 μs switching delay is observed for full 2 V output. Using this inverter, we also attempted to form NAND and NOR logic gates as seen in figures 6(a) and (c), where two different inputs (IN1 and IN2) are employed for circuit operation. For NAND operation, neighbor gate is selected as IN2 beside the driver gate of inverter (IN1) while for NOR application, another FET gate located across the space between two FET arrays is selected as IN2. Figures 6(b) and (d) nicely demonstrate the time domain operation of NAND and NOR logic functions. Based on aforementioned MoS_2 FET, NOT, NAND, and NOR logic integrated circuits, we now regard that our CVD-grown MoS_2 and its transfer method is quite

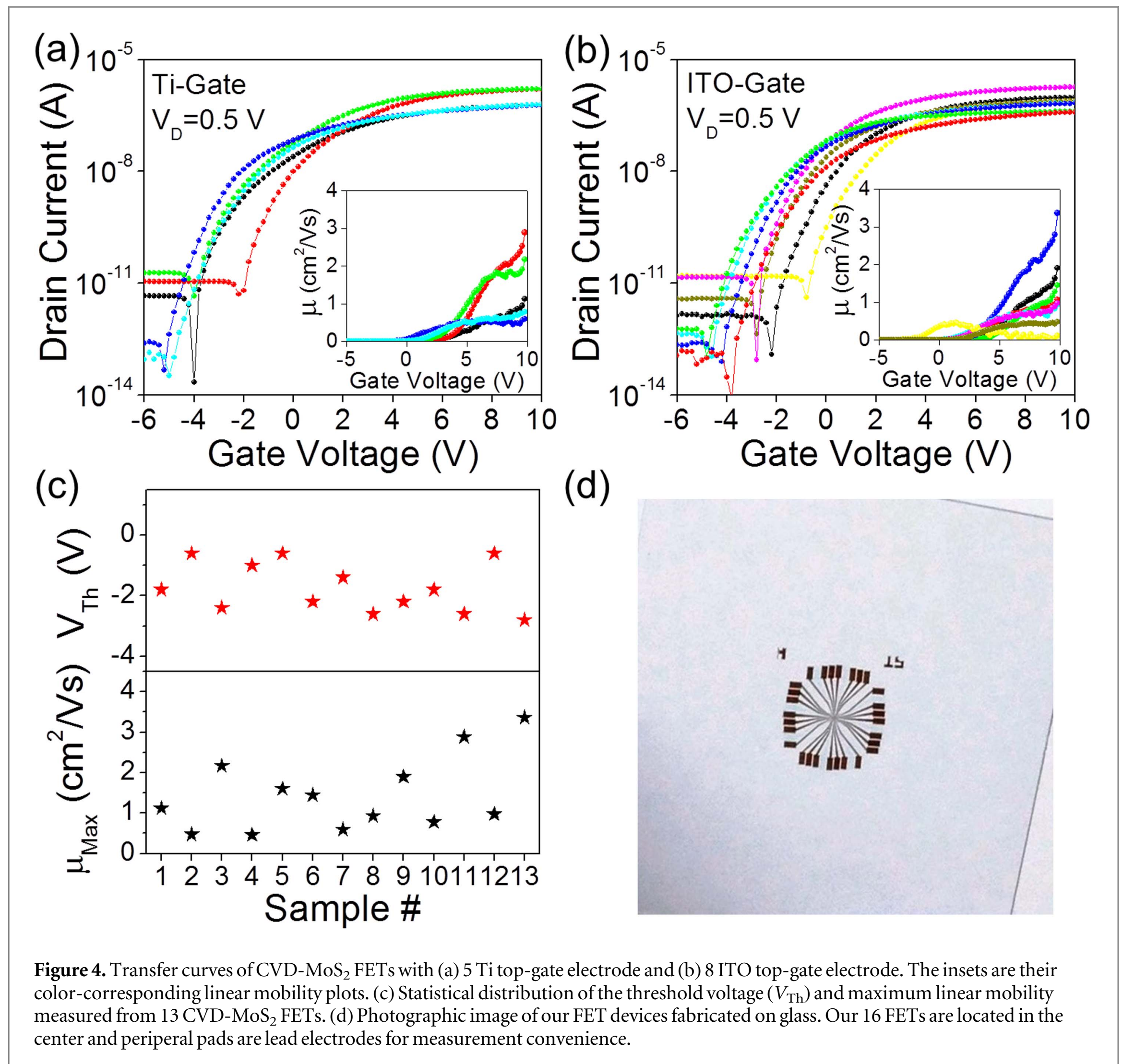

Figure 4. Transfer curves of CVD-MoS_2 FETs with (a) 5 Ti top-gate electrode and (b) 8 ITO top-gate electrode. The insets are their color-corresponding linear mobility plots. (c) Statistical distribution of the threshold voltage (V_{Th}) and maximum linear mobility measured from 13 CVD-MoS_2 FETs. (d) Photographic image of our FET devices fabricated on glass. Our 16 FETs are located in the center and periperal pads are lead electrodes for measurement convenience.

useful for full photolithography-patterned large scale 2D circuit integrations.

3. Conclusion

In summary, we have fabricated CVD-grown 2D MoS_2 FET and logic circuits on glass substrate by PMMA-induced flake transfer and photolithography, aiming at 500 × 500 μm^2 large scale circuit integration. Maximum linear mobility of our single-domain MoS_2 FET was ~9 $cm^2 V^{-1} s^{-1}$ on SiO_2/p^+–Si substrate but appears reduced to be 0.5~3 $cm^2 V^{-1} s^{-1}$ on glass due to the loss of back channel [31–35], transfer process-induced wrinkles [23, 24], domain boundaries [25–28], and chemical residue on MoS_2 [29, 30]. Among 16 MoS_2-based FETs, 13 devices successfully operate, being able to produce NOT, NOR, and NAND logic circuits. Inverter (NOT gate) shows quite a high voltage gain over 12 at a supply voltage of 5 V, also displaying 60 μs switching speed in kilohertz dynamics. We conclude that our large scale MoS_2 circuit integration by full photolithography and flake transfer is promising enough to open a new gate for future large area flexible or transparent electronics using 2D semiconducting materials although flawless flake transfer remains as a further study.

4. Experimental section

4.1. MoS_2 CVD growth

MoS_2 films in this study were grown by CVD system (Tenaleader CO., Ltd). Our CVD system is composed of dual-heating zones; one heating zone is for Sulfur powder (99.98%, Aldrich) and the other is for MoO_3 powder (99.5%, Aldrich) and SiO_2 substrates. We used substrates which have thermally oxidized 270 nm SiO_2 on highly p-doped silicon. These substrates were cleaned in acetone, 2-propanol for 5 min separately. Lastly, we did ultraviolet ozone cleaning for 5 min. And these substrates were located upside-down with MoO_3 powder (~10 mg) on a quartz boat. The sulfur powder (~400 mg) is on a different quartz boat. The sulfur and tri-oxide zones are heated up to ~150 °C and ~700 °C each. In order to remove the

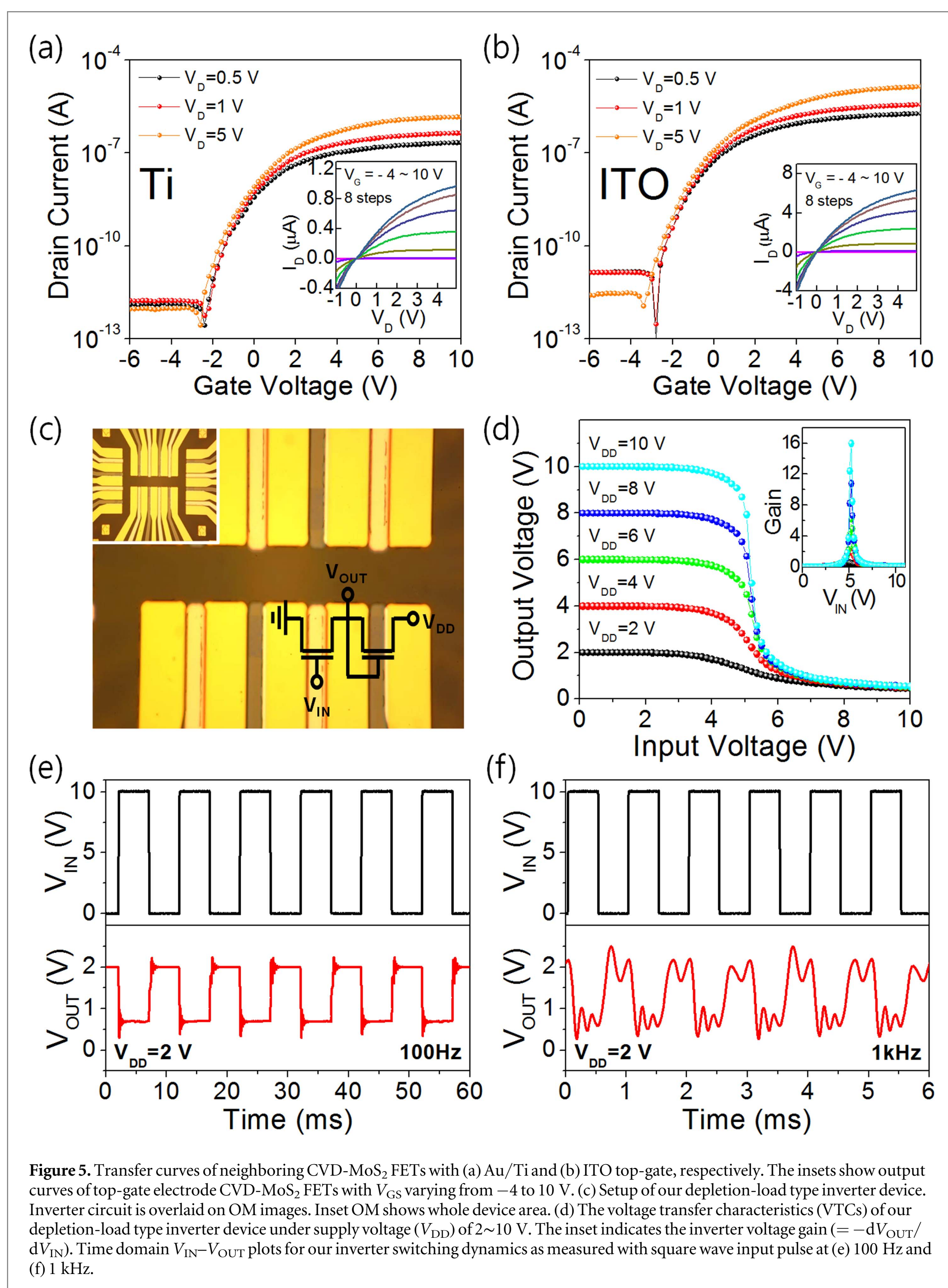

Figure 5. Transfer curves of neighboring CVD-MoS_2 FETs with (a) Au/Ti and (b) ITO top-gate, respectively. The insets show output curves of top-gate electrode CVD-MoS_2 FETs with V_{GS} varying from −4 to 10 V. (c) Setup of our depletion-load type inverter device. Inverter circuit is overlaid on OM images. Inset OM shows whole device area. (d) The voltage transfer characteristics (VTCs) of our depletion-load type inverter device under supply voltage (V_{DD}) of 2~10 V. The inset indicates the inverter voltage gain ($= -dV_{OUT}/dV_{IN}$). Time domain V_{IN}–V_{OUT} plots for our inverter switching dynamics as measured with square wave input pulse at (e) 100 Hz and (f) 1 kHz.

contaminants inside the quartz tube, we purged the quartz tube with Ar gas for 1 h (500 sccm) after loading all the ingredients. And then inside the quartz tube was painted as 10 Torr (10 sccm) for the entire growth process.

4.2. Transfer process

As-grown MoS_2 on SiO_2/p^+–Si substrate was spin-coated with PMMA (MW = 950000, Sigma-Aldrich) at 3000 rpm for 30 s. The sample was annealed at 180 °C for 2 min. The SiO_2/p^+–Si substrate was dipped into KOH solution (0.449 g ml^{-1}) at room temperature for 5~6 h to etch SiO_2 layer, so that the PMMA/MoS_2 membrane was floated on the surface of the solution. The PMMA/MoS_2 membrane was washed with deionized water and placed on the glass for drying. After the transfer to the glass, the PMMA residues were removed using acetone. The schematics of transfer process are illustrated as figure 2(a) in detail.

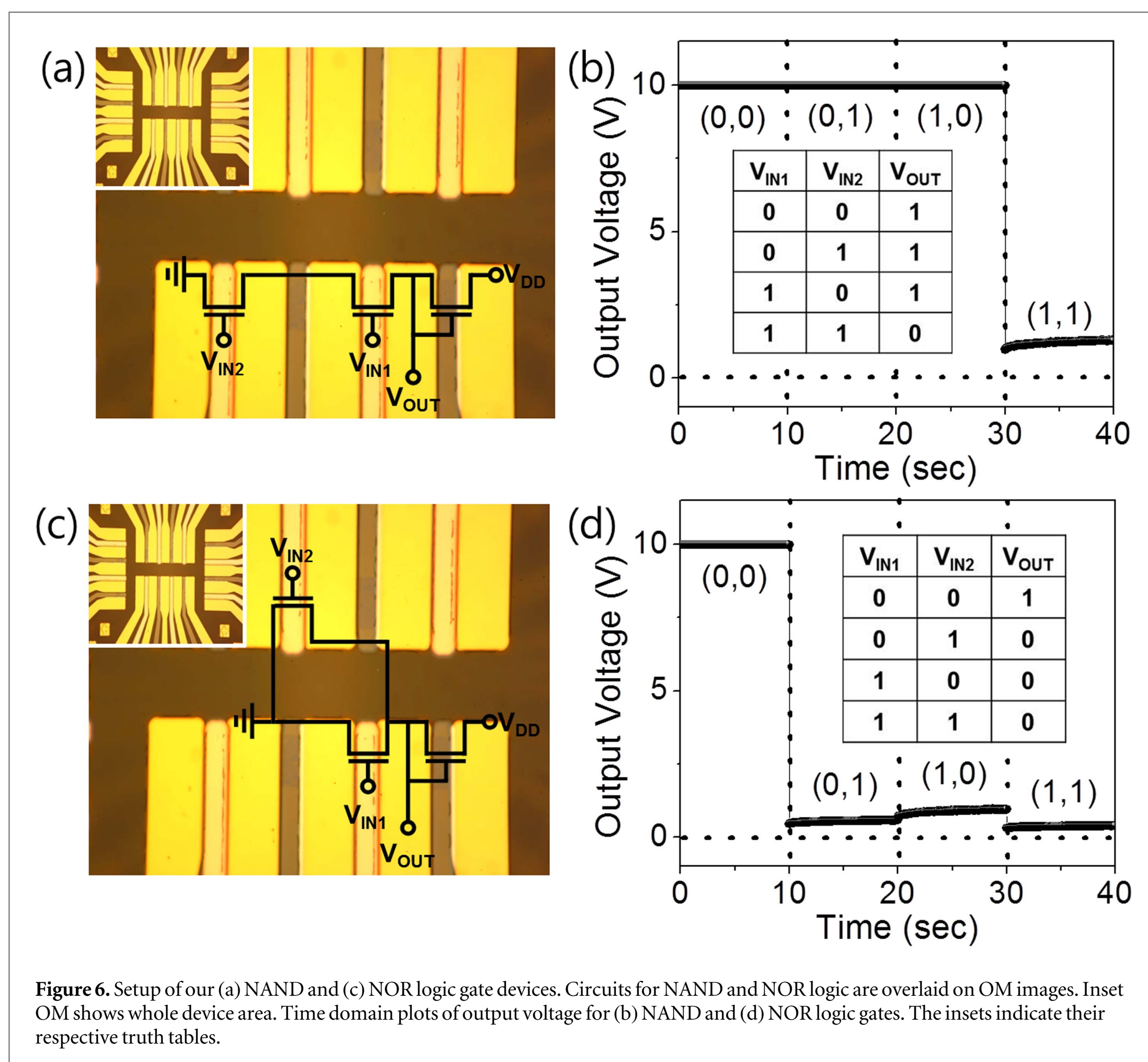

Figure 6. Setup of our (a) NAND and (c) NOR logic gate devices. Circuits for NAND and NOR logic are overlaid on OM images. Inset OM shows whole device area. Time domain plots of output voltage for (b) NAND and (d) NOR logic gates. The insets indicate their respective truth tables.

4.3. Device fabrication

The CVD-grown MoS_2 flakes were patterned by photolithography and O_2 plasma dry etching process with photoresist layer (AZ GXR-601, AZ electronic materials). For the patterning of our large area MoS_2 flakes, lift-off layer (300 nm) (LOR 3 A, Micro Chemical) and 1.3 μm-thick photoresist (PR) layer were initially spin-coated at 1000 rpm for 10 s (step 1) and 3000 rpm for 30 s (step 2). Then, lift-off layer and photoresist were baked on hot plate at 140 °C and 100 °C for 2 min respectively. After spin coating, we exposed UV light for 2 s using photomask aligner (MDA-400S, MIDAS SYSTEM CO., Ltd) and developed the PR layer for 65 s. Plasma etching process was performed at flow rate of 10 sccm oxygen and 150 W for 3 min in a plasma etching system (CUTE-MP, FEMTO SCIENCE). For the patterning of source (S) and drain (D) ohmic contact electrodes, Au/Ti (50/25 nm) were deposited by DC magnetron sputtering system while those were patterned by photolithography and lift-off process with lift-off layer and photoresist layer. Then, the device was annealed at 250 °C with N_2 flow in rapid thermal anneal (RTA) system for 10 min to remove polymer residue and simultaneously to reduce contact resistance. For dielectric layer, 50 nm of Al_2O_3 layer was deposited at 100 °C by atomic layer deposition (ALD) system using H_2O reactant molecules. The opaque Au/Ti (50 nm/25 nm) bilayer and transparent ITO (75 nm) single layer were deposited and patterned for their top gate (G)-electrodes, respectively by the same photolithography process as that for S and D. The channel width/length ratios were defined to be 12 μm/5 μm for our CVD-MoS_2 FETs. (More details for device fabrication are seen as a step-by-step order in supplementary information).

4.4. Measurements

The device current–voltage (I–V) characterizations were carried out by a semiconductor parameter analyzer (HP 4155 C, Agilent Technologies). Electrical dynamics measurements were investigated with a function generator (AFG 310, Sony/Tektronix) and an oscilloscope (TDS210, Tektronix). The topographic image of CVD-MoS_2 on SiO_2/p^+–Si and glass substrate was characterized by atomic force microscope (AFM, Nanowizard I, JPK Instrument). SEM images were taken with an Field Emission Scanning Electron Microscope (SEM, JSM-7001F, JEOL Ltd). The exact number of layers for each CVD-MoS_2 was characterized by Raman spectroscopy (LabRam Aramis, Horriba Hovin Yvon).

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