

Gate-dependent asymmetric transport characteristics in pentacene barristors with graphene electrodes

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Received 19 April 2016, revised 10 September 2016

Accepted for publication 22 September 2016

Published 21 October 2016



CrossMark

Abstract

We investigated the electrical characteristics and the charge transport mechanism of pentacene vertical hetero-structures with graphene electrodes. The devices are composed of vertical stacks of silicon, silicon dioxide, graphene, pentacene, and gold. These vertical heterojunctions exhibited distinct transport characteristics depending on the applied bias direction, which originates from different electrode contacts (graphene and gold contacts) to the pentacene layer. These asymmetric contacts cause a current rectification and current modulation induced by the gate field-dependent bias direction. We observed a change in the charge injection barrier during variable-temperature current–voltage characterization, and we also observed that two distinct charge transport channels (thermionic emission and Poole–Frenkel effect) worked in the junctions, which was dependent on the bias magnitude.

 Online supplementary data available from stacks.iop.org/NANO/27/475201/mmedia

Keywords: graphene, pentacene, thermionic emission, Poole–Frenkel conduction, barristor

(Some figures may appear in colour only in the online journal)

1. Introduction

Since its discovery, graphene has attracted considerable attention due to its advantageous properties, such as high carrier mobility, good mechanical properties, and chemical stability [1–6]. However, graphene has a fundamental limitation for use as an active channel in semiconductor devices such as field effect transistors (FETs) because of its zero-band gap feature. However, graphene's outstanding features of high conductivity, good flexibility, and transparency have led

to it being explored for use as an electrode in various electrical and optical devices, including FETs [7–9], light-emitting diodes (LEDs) [10, 11], and photovoltaic devices [12, 13]. For example, Han *et al* demonstrated flexible organic LEDs with extremely high luminous efficiency by introducing graphene sheets with a high work function in place of the conventional indium tin oxide electrodes [11]. We also previously demonstrated that pentacene organic thin film transistors (OTFTs) with graphene electrodes exhibited an enhanced charge injection property with a reduced contact resistance compared to devices with typical Au electrodes [8].

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In most cases, OTFTs are fabricated in the form of a horizontal FET device structure, in which two side regions across the organic channel layer are contacted by the source and drain electrodes from the bottom or from the top (called bottom-contact or top-contact OFETs, respectively). In contrast, alternative vertical structures of FET devices with graphene electrodes have been demonstrated. The vertically stacked FET structure consists of gate/oxide/graphene/semiconductor/metal, and it is called a vertical FET (VFET) or barristor, in which a graphene film and metal (or another graphene film) are used as the bottom and top electrodes, respectively [14–17]. The charge injection barrier built within the graphene/channel interface can be effectively modulated by the electric field induced by the gate bias because the Fermi level of the semiconductor layer is not pinned to the Fermi level of graphene. Various semiconducting materials, such as silicon, molybdenum disulfide (MoS_2), tungsten disulfide (WS_2), and amorphous indium gallium zinc oxide (α -IGZO), have been utilized in the VFET structure and exhibited a decent current modulation by the gate bias. For example, MoS_2 VFETs with graphene electrodes showed transistor action with an on–off current ratio of 10^1 – 10^3 depending on the channel thickness at room temperature [16]. Organic films have also been applied as the channel in graphene-electrode VFET devices [18–21]. Ojeda-Aristizabal *et al* demonstrated gate tunability in pentacene ‘barristor’ with graphene electrodes [18]. These authors demonstrated a gate-induced current modulation with a factor of 4 in response to changes in the gate bias from -50 to 50 V. Although a preliminary study of the electrical characteristics of graphene-electrode pentacene barristor has been performed, a more thorough analysis and understanding are desired, particularly in terms of the effect of asymmetric barrier contacts in the graphene/pentacene/Au barristor structure.

Herein, we independently investigated pentacene barristors with graphene and Au electrodes. We measured and analyzed the electrical transport characteristics of the barristors by focusing on the properties originating from the asymmetric electrical contacts in the graphene/pentacene/Au structure. We also investigated the conduction mechanisms by considering the contribution of the bias voltage applied between graphene and Au and gate bias to the activation energies of interfacial trap sites.

2. Experimental details

2.1. Device fabrication process

Figure 1(a) presents optical microscopy and scanning electron microscopy images of the pentacene barristors, and figure 1(b) presents a schematic image of the device structure. These devices consist of vertical heterojunction of graphene/pentacene/Au on Si/SiO₂ substrate. We fabricated this pentacene barristors by following procedures. First, we prepared a silicon substrate ($1.5\text{ cm} \times 1.5\text{ cm}$) of a 270 nm thick SiO₂ layer on a heavily doped p⁺⁺ Si wafer (resistivity $\sim 5 \times 10^{-3}\ \Omega\text{ cm}$) that can be used as a back gate. Au (30 nm

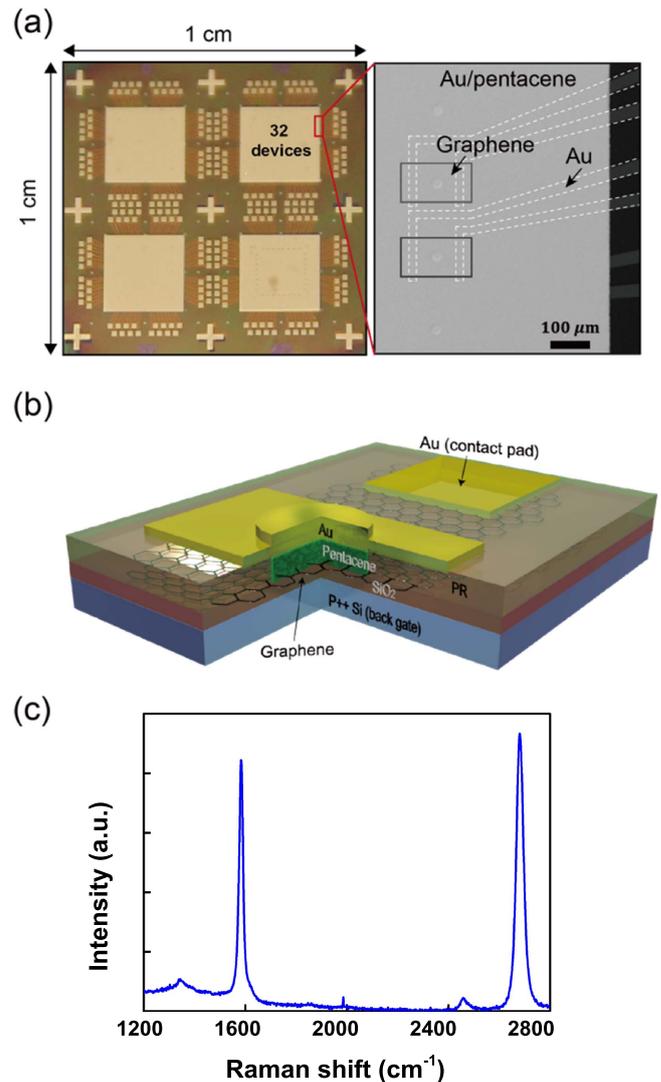


Figure 1. (a) The optical microscopy image (left) and scanning electron microscopy image (right) of the pentacene barristors. (b) The schematic image of the pentacene barristor. The bias voltage is applied to the graphene electrode, and p⁺⁺ Si serves as the gate electrode. (c) Raman spectrum of the graphene film used as an electrode of the device.

thick)/Ti (5 nm thick) metal layers were deposited and patterned on the substrate using an e-beam evaporator and a conventional photo-lithography technique, which will be used as a probing pad for the graphene electrode film. For the graphene electrode film, a single-layer graphene sheet was grown on a Cu foil ($\sim 10\text{ cm} \times 10\text{ cm}$) using the chemical vapor deposition (CVD) method. The grown graphene sheet was detached from the Cu foil using a wet transfer process and transferred to the substrate that contained pre-patterned Au contact pads. We patterned the transferred graphene sheet into small rectangular-shaped patches ($200\ \mu\text{m} \times 100\ \mu\text{m}$, black line in figure 1(a), right) using photolithography and oxygen plasma etching processes to create the desired contacts with the Au contact pads. Figure 1(c) shows the Raman spectrum of a graphene film that was transferred onto a Si/SiO₂ substrate. The Raman data suggest that the synthesized

graphene film is a monolayer graphene film. Defect generated in synthesis or transferring process may be responsible for the rather high G peak compared to the 2D peak. Note that water or oxygen attached on graphene could work as defects so the graphene layer slightly exhibited p-type behaviors. Next, the isolation wall was created with a photoresist (PR) layer (AZ5214) by photolithography. This PR wall was created for preventing a direct charge pathway between bottom and top electrodes. We created vertical holes with a radius of 10 μm such that the graphene was revealed. Following this process, Pentacene (500 nm thick) was deposited on the substrate using a thermal evaporator at a rate of $\sim 0.5 \text{ \AA s}^{-1}$. Finally, the top Au (50 nm thick) electrode was formed on the pentacene layer using an e-beam evaporator and shadow masks.

2.2. Device characterization

We measured all the electrical characteristics of the pentacene barristors with the temperature-variable probe station (JANIS, ST-500) and the semiconductor parameter analyzer (Keithley, 4200-SCS) under vacuum condition ($\sim 1 \text{ m Torr}$). The temperature cooled down by supplying the liquid nitrogen. The Au top electrode was connected to ground and the bias voltage (V_b) was applied between the top and bottom electrodes. The current measured at the graphene bottom electrode (I_b).

3. Results and discussion

3.1. Asymmetric charge transport properties

Figures 2(a) and (b) show the representative current–voltage characteristics of a graphene-electrode pentacene barristor at room temperature. Figure 2(a) shows the output characteristics (the current versus the bias voltage; I_b – V_b) at various gate bias voltage (V_g) ranging from -80 V to 80 V with an interval of 20 V . In this plot, diode-like electrical characteristics were observed, that is, there was a larger current flow under positive V_b compared to that under negative V_b at zero gate bias. In addition, significant current modulation by gate bias was observed only in positive V_b . Figure 2(b) presents the transfer curves (the current versus gate bias; I_b – V_g) at two fixed V_b values of $\pm 9 \text{ V}$. The current at the V_b of $+9 \text{ V}$ (red line) decreased when the gate bias increased. It should be noted that current modulation was dominantly attributed to the change of the Schottky barrier height by gate bias. In contrast, the current at the V_b of -9 V (black line) did not significantly change. This voltage-dependent asymmetric property originates from the vertical heterostructure of the graphene/pentacene/Au stack, in which the charge transport is affected by the energy barrier at the top contact (with Au) and bottom contact (with graphene) of pentacene. In particular, current modulation was observed at specific bias voltage range ($V_b > 0 \text{ V}$) because only the barrier height at the graphene/pentacene interface was effectively varied by the gate field due to the low density of states of graphene near the Dirac point in contrast to the barrier at the interface adjacent to Au, which has numerous densities of states.

To investigate the rectifying property, we defined the rectification ratio (R) as the ratio between I_b (at positive V_b) and I_b (at negative V_b) and analyzed it within various V_g and V_b at room temperature. This result is shown in figure 2(c). The current rectification ratio increased up to 2.8 as $|V_b|$ increased and V_g decreased. The graphene electrode has remarkable advantages in aspect of the formation of distinct dipole layers compared to the use of the Au electrode built on each interface [8]. Pentacene, a p-type organic semiconductor, has its highest occupied molecular orbital (HOMO) located near the Fermi level of each electrode material, and thus, hole transport determines the current flow of this device. The pentacene layer deposited on graphene is stacked in a planar orientation through π – π interactions with graphene [22]. In this case, the interfacial dipole is formed at the graphene/pentacene junction interface such that it elevates the vacuum level of pentacene, resulting in lowering of the hole injection barrier [23, 24]. In contrast, the dipole layer formed at the pentacene/Au junction interface raises the hole injection barrier [25, 26]. The holes transport from the graphene to pentacene in the positive V_b range; thus, relatively large current flows due to the lowered hole injection barrier. Similarly, in the negative V_b range, a smaller current flows because of the increased hole injection barrier from the Au to pentacene. The exact energy barrier height can be estimated from variable-temperature electrical measurement, which will be discussed in a later section. This rectification ratio is also modulated as V_g varied because the current modulation occurs only in the positive V_b range (see figure 2(b)). This gate-dependent rectification can be clearly observed in the inset of figure 2(c), in which the rectification ratio was calculated as a function of V_g at a fixed $|V_b| = 8 \text{ V}$. Note that the rectification ratio linearly increased with $|V_b|$ but saturated above a certain bias voltage, as indicated by the black dashed line in figure 2(c).

3.2. Barrier height modulation by the gate field

To further investigate the phenomena for the asymmetric properties in the current–voltage and current modulation characteristics, we conducted variable-temperature current–voltage (I – V – T) measurements while the temperature was changed from 220 to 280 K in increments of 10 K. The current modulation under various V_b and temperature conditions are presented in figure 2(d), in which the ON/OFF ratio was defined as the ratio of I_b ($V_g = -80 \text{ V}$)/ I_b ($V_g = 80 \text{ V}$). The ON/OFF ratio in the negative V_b range remained invariant due to little current modulation. However, for the positive V_b range, this ratio increased up to ~ 50 in the low temperature and low bias voltage region. The graphene/pentacene/Au stack can be considered to be two Schottky diodes reversely connected to each other. If the pentacene layer is fully depleted, then the Schottky barrier over which charge carriers inject from the electrode to pentacene determines the electrical characteristics of the entire junction [16, 27, 28]. Figures 3(a) and (b) show Arrhenius plots ($\ln(I_b/T^2)$) versus $q/k_B T$ for various gate biases from -80 to 80 V at a fixed V_b of $\pm 2 \text{ V}$. A linear dependency was observed in these plots,

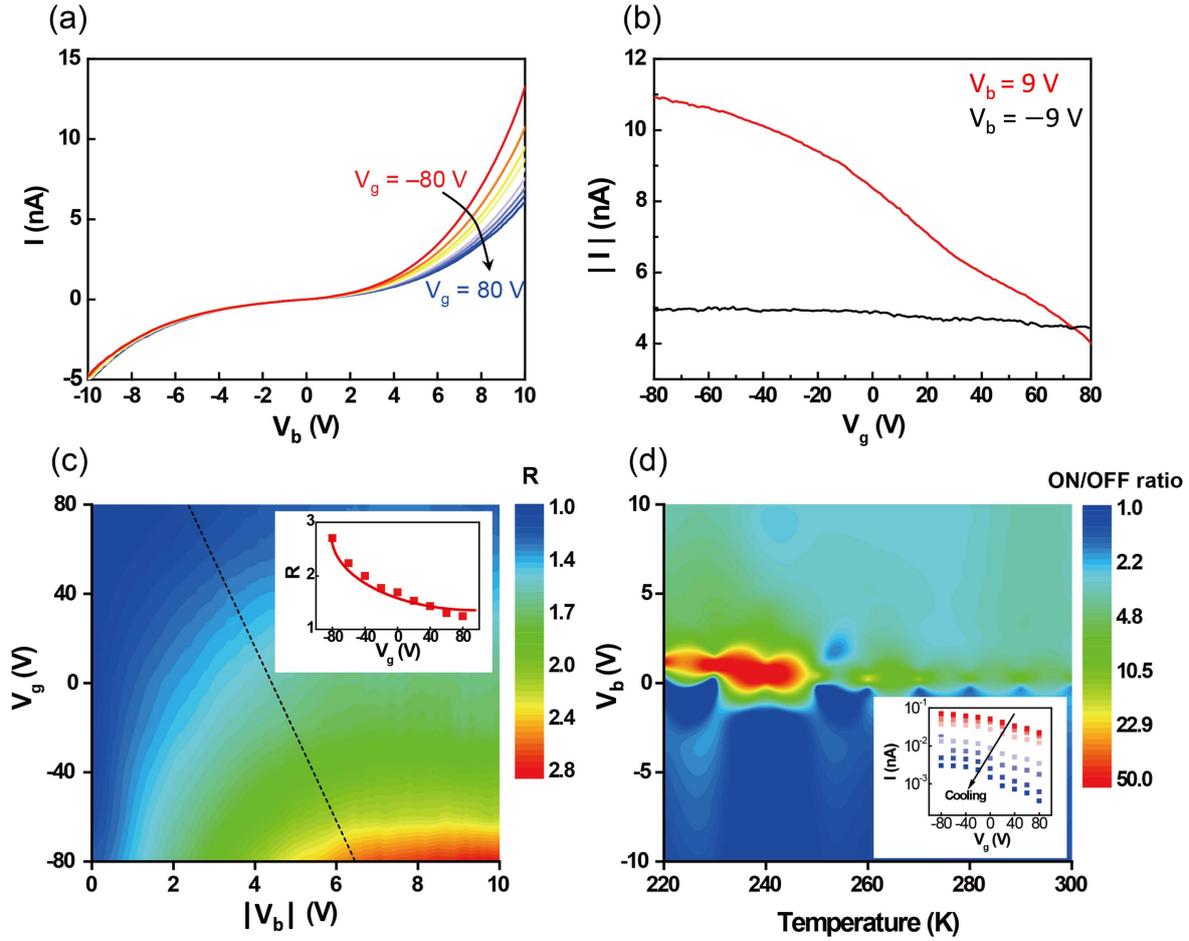


Figure 2. (a) The output characteristics (I_b - V_b) with V_b ranging from -10 V to 10 V at various V_g . (b) The transfer curves (I_b - V_g) of pentacene barristor at $V_b = \pm 9$ V. Both characteristics were measured as V_g increased from -80 V to 80 V. (c) Contour plot of the rectification ratio $R = I_b(V_b > 0)/I_b(V_b < 0)$ within given V_b and V_g . The inset shows R versus V_g at $V_b = 8$ V. At fixed V_g , R was saturated in V_b higher than the values that are presented with a black dashed line. (d) Contour plot of ON/OFF ratio obtained from the I - V - T measurement. The inset shows transfer curves at various temperature conditions.

which implies that the device obeys the thermionic emission as

$$I_b = AA^*T^2 \exp\left(-\frac{\phi_s - qV_b}{k_B T}\right), \quad (1)$$

where A is the junction area, A^* is the effective Richardson constant, q is the elementary charge, k_B is the Boltzmann constant, and ϕ_s is the Schottky barrier height (i.e., the difference between the Fermi level of the electrode and the HOMO level of pentacene) that the holes cross over from the electrode to pentacene. Therefore, the slopes of the fitting lines in right and left part of figure 3(a) are related to the Schottky barrier at the graphene/pentacene and pentacene/Au interfaces, respectively. From these figures, one can observe that the slope, that is, the energy barrier, changed more by the gate bias at positive V_b (here, 2 V), whereas the slopes of the Arrhenius plots did not change noticeably by the gate bias at negative V_b (here, -2 V). Although the bias voltage applied to the graphene bottom electrode affects the strength of electric field from the gate contact (i.e., by screening the gate electric field), this screening effect by the graphene electrode can be negligible because of the relatively

small V_b compared to the large gate bias (up to 80 V). Figure 3(b) summarizes the energy barrier (ϕ_s) modulation induced by the gate bias, extracted from the slopes of the fitting lines in figure 3(a). As shown in this plot, the barrier height changed from 220 to 320 meV at positive V_b , whereas only a negligible change was found for negative V_b . In the $V_b > 0$ range, in which the holes are injected into pentacene from the graphene electrode, the charge injection barrier that the holes have to pass through was tuned by the gate field, and thus, the current in the $V_b > 0$ range is modulated. It should be noted that the dominant mechanism for current modulation in this device is the change of the carrier injection barrier by the gate bias, not the change of the pentacene channel conductivity. The result of I - V - T measurement is consistent with the high ON/OFF ratio at low temperature in figure 2(d) because this ratio is proportional to the exponential of $\Delta\phi_s/k_B T$, where $\Delta\phi_s$ is the energy barrier height variation in the given gate bias range. Moreover, note that the gradient of the energy barrier height was larger at low gate bias. This result implies that the Dirac point of graphene with the lowest density of states (DOS) also existed at low gate bias. The gradient tended to decrease as the gate bias increased because

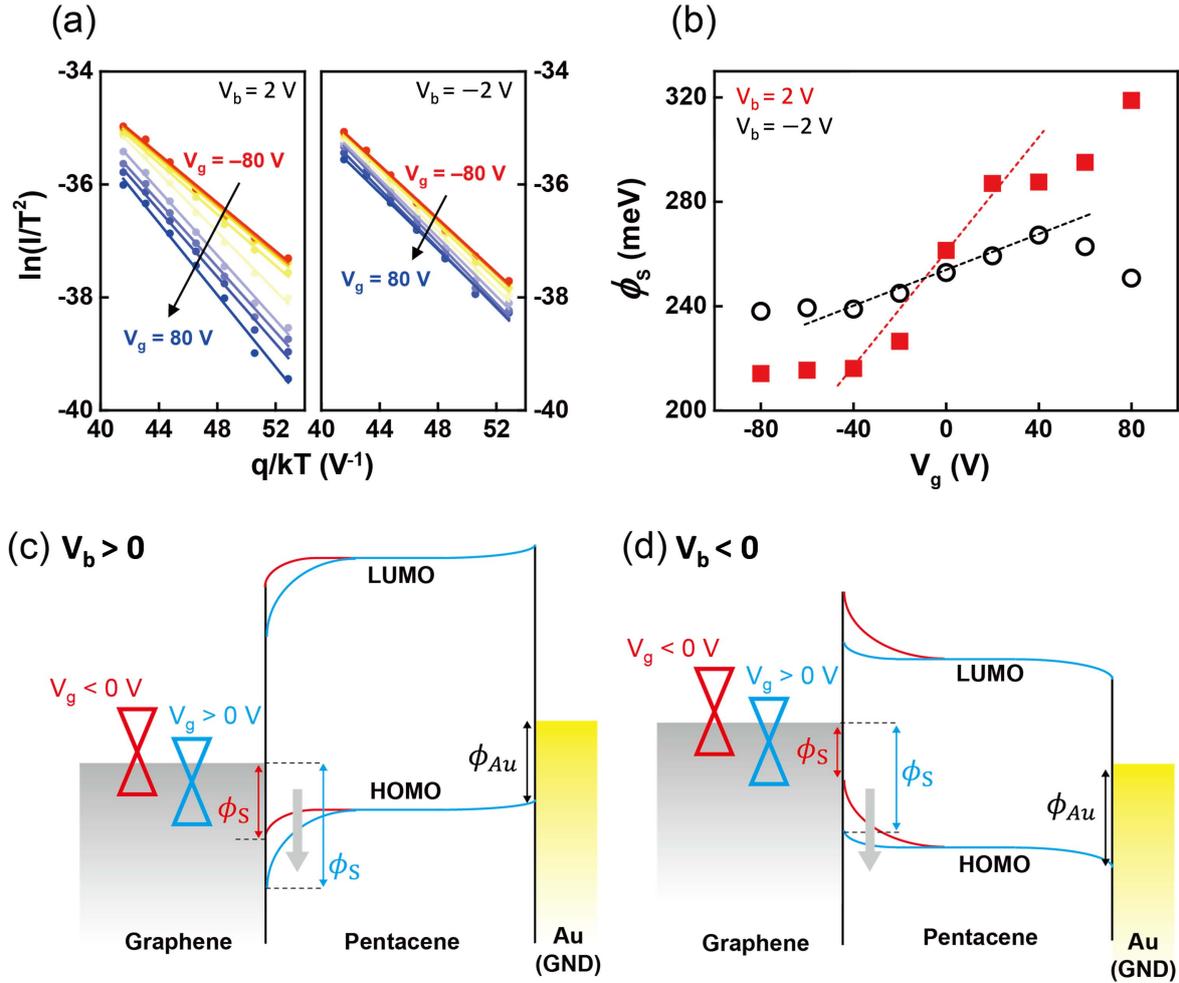


Figure 3. (a) Arrhenius plots at $V_b = 2$ V (left) and at $V_b = -2$ V (right), in which the slopes of each line correspond to the Schottky barrier height (ϕ_S). (b) Schottky barrier modulation by gate bias voltage at $V_b = 2$ V (red squares) and at $V_b = -2$ V (black circles). The dashed lines are the gradient of ϕ_S near $V_g = 0$ V. (c), (d) The schematic band diagrams in the range of (c) $V_b > 0$ and (d) $V_b < 0$. The energy bands are expressed as red lines for $V_g < 0$ and blue lines for $V_g > 0$.

the more carrier density was induced, resulting in more DOS in the graphene. Note that Ojeda-Aristizabal *et al* also previously observed ϕ_S modulation of ~ 300 meV in a similar pentacene barristor structure [18]. In our study, we observed ϕ_S modulation of ~ 100 meV (difference of 220 and 320 meV). This difference may be related to the different quality of graphene used. Unlike pristine graphene obtained using the mechanical exfoliation method, the graphene used in this study, which was synthesized using CVD, may have more defect sources, such as grain boundaries, wrinkles, or PMMA residues [29–31], inducing unintended interface states at the graphene/pentacene junction. This may weaken the Fermi level unpinning of pentacene and disturb the energy barrier modulation.

In contrast to the apparent current modulation in positive V_b range, it is extremely limited in negative V_b range due to the negligible change of the barrier height at the interface between Au electrode and pentacene layer. The numerous DOS of Au contrary to graphene can be one of origins of this behavior. The weakened field by the induced carrier density in the graphene electrode can be another reason.

We observed that the energy barrier height variation ($\Delta\phi_S$) in the given gate bias range monotonically decreased as the bias voltage increased (see figures S2 and S3 in the supplementary materials). This result indicates that the contribution of the gate field to the current modulation decreased as the bias voltage increased, and it also suggests that another charge transport channel rather than thermionic emission occurred at high V_b range, which will be further explained later.

The schematic energy band diagrams of the pentacene barristor that can explain the above results are presented in figures 3(c) and (d). When a positive voltage is applied to the graphene electrode, the hole carriers flow from graphene into the junction, passing through the energy barrier at the graphene/pentacene contact (figure 3(c)). In this case, the I_b – V_b relation is approximated using equation (1), where ϕ_S is the Schottky barrier height in the graphene/pentacene interface. The gate field effectively tunes this injection barrier because the Fermi level of pentacene is not pinned to the Fermi level of graphene due to its low density of states and small number of electrons near the Dirac point. Under the positive V_b

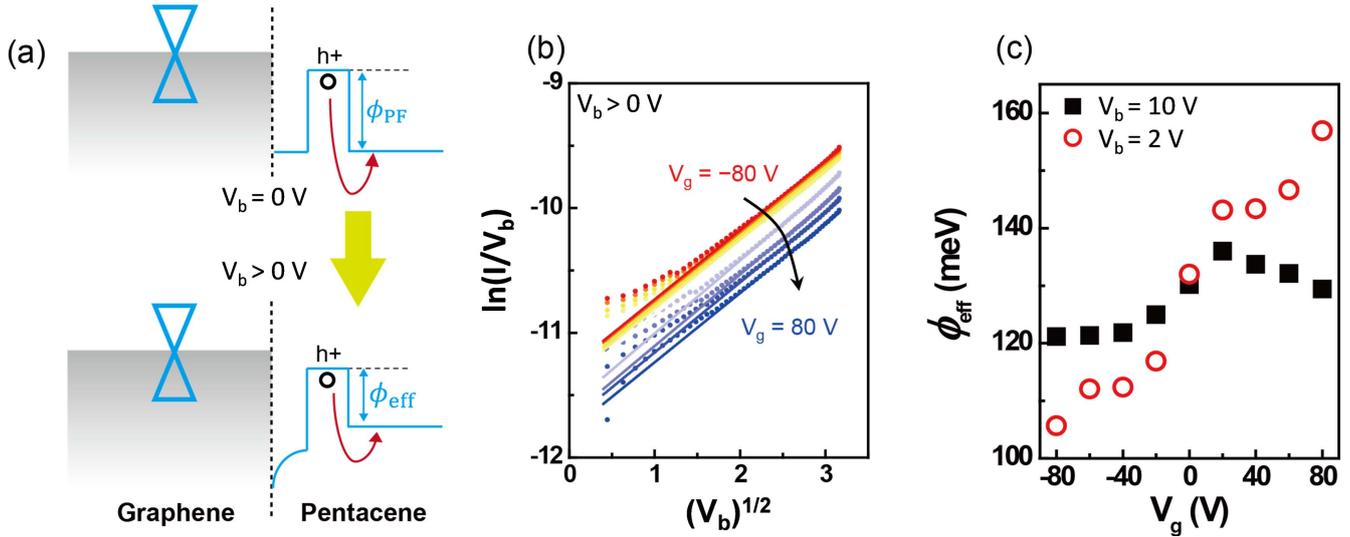


Figure 4. (a) The band diagram corresponding to the Poole–Frenkel model (upper) when zero field and (lower) a finite field is applied. The hole injects to trap sites and transports through the valence band of pentacene. (b) Plot of $\ln(I_b/V_b)$ versus V_b in various V_g in which the Poole–Frenkel conduction is featured as linear fitting in the high V_b range. (c) The modulation of effective barrier height (ϕ_{eff}) of trap sites in non-zero field situation by gate bias voltage at $V_b = 2$ V (red circles) and at $V_b = 10$ V (black squares).

condition, the negative gate bias voltage elevates the energy bands of both graphene and pentacene. Therefore, hole-rich graphene and the reduced barrier lead to the large current flow. When a positive gate bias is applied, the charge transport is restrained due to the increased energy barrier at the graphene/pentacene contact. In contrast, if a negative V_b is applied, then the hole carriers flow from the Au top electrode to the pentacene layer, and thus, the Schottky barrier in the Au/pentacene interface (ϕ_{Au}) is involved in the charge transport (figure 3(b)). In this case, the Fermi level of pentacene pinned to the Fermi level of Au, and the corresponding energy barrier heights are hardly changed by the unscreened gate electric field penetrating the graphene/pentacene layer. Therefore, the current at the negative V_b range remains almost constant while the gate bias is changed.

3.3. Bias-dependent current modulation

To understand the $\Delta\phi_S$ dependence on bias, we investigated another type of charge transport through this heterojunction, namely, the Poole–Frenkel (PF) model, which describes the conductance in materials with localized trap sites by a charge trapping/de-trapping process [32, 33]. As shown in the upper part of figure 4(a), if there are trap sites in the interface or bulk, then holes can be captured in the potential well with a depth of ϕ_{PF} when zero field is applied through the junction, and this potential well depth is reduced by an electric field. As the finite electric field is applied, holes tunnel from the electrode to the localized states. Then, holes with sufficient thermal activation energy are able to transport along the valence band by escaping the potential well. The PF model also illustrates how the electric field applied in material reduces the potential well of trap sites as the following

equation

$$I_b \propto E \exp\left(-\frac{\phi_{\text{PF}} - q\sqrt{qE/(\pi\epsilon)}}{k_B T}\right), \quad (2)$$

where E is the applied electric field within the trap site that reduces the effective barrier height for charge carriers to move into the valence band and ϵ is the permittivity of the material. The effective barrier height (ϕ_{eff}) described in the lower part of figure 4(a) is the potential well height reduced by the finite field, i.e., $\phi_{\text{eff}} = \phi_{\text{PF}} - q\sqrt{qE/(\pi\epsilon)}$. If the charge transport of our device follows the PF model, then the $\ln(I_b/V_b)$ versus V_b curves would show the linearity because E is given as V_b/d_p , where d_p is the thickness of pentacene (500 nm). Figure 4(b) presents the $\ln(I_b/V_b)$ versus $\sqrt{(V_b)}$ plots of the pentacene barristor at various gate biases. These curves show the linear relation only in the high bias voltage range ($V_b > 3$ V), which means that the PF model can be applied to the device in the high field region. However, this plot shows a nonlinear trend when a low bias voltage ($V_b < 3$ V) is applied. This deviation from linearity implies that thermionic emission becomes more important as the bias is lowered. We note that the gate field also contributes to this deviation because the starting points of ‘tails’ (part deviating from the trend lines) and their deviations are dependent on V_g . This is reasonable because the charges are injected to pentacene over the Schottky barrier modulated by the gate field in the thermionic emission model, which is the dominant transport mechanism in the low bias range. The effective barrier height (ϕ_{eff}) within the pentacene–graphene interface in a finite electric field can be extracted from the I – V – T measurement as the slope of the $\ln(I_b/E)$ versus \sqrt{E} plot. Here, we consider the field induced by V_g and V_b as $E = V_b/d_p + V_g/d_{\text{ox}}$, where d_p and d_{ox} are the thicknesses of the pentacene layer (500 nm) and SiO_2 (270 nm), respectively, and the portion of the gate field weakly screened by induced charge on the

graphene sheet is neglected in this calculation. The result is illustrated in figure 4(c). It is clear that the gate field dependence of ϕ_{eff} is stronger at low bias ($V_b = 2$ V) than at high bias ($V_b = 10$ V). This result supports the inference that the PF model is an important charge transport mechanism in our device structure. Because the gate field occupies a significant portion of the field within the graphene–pentacene interface when a low bias is applied, ϕ_{eff} is effectively modulated by the gate bias voltage, while ϕ_{eff} only shows a very small change at high V_b , where the gate field is negligible compared to the field induced by the bias voltage. The low ON/OFF ratio in the high V_b region can also be explained in this context; because the field induced by the bias voltage contributes to barrier height modulation considerably more than the gate field, the current cannot vary effectively. We also observed that the slopes of the trend lines for the high-temperature range ($T > 280$ K) in the Arrhenius plots are hardly affected by the gate bias (figure S4), which is further support for the PF model [32, 34].

4. Conclusions

In summary, we fabricated and characterized graphene/pentacene/Au vertical hetero-structure. These devices have unique electrical properties compared to conventional (planar) pentacene thin film transistors. The current–voltage curves were nonlinear and asymmetric, and they showed larger current flow in the positive bias voltage range. The current modulation induced by the gate field was also asymmetric. We conducted variable-temperature measurements and demonstrated that these electrical characteristics originated from the different energy barrier properties at the graphene–pentacene and pentacene–Au contacts. The charge transport within this heterojunction is attributed to thermionic emission and the PF model, which is consistent with the results of a previous study [18, 33]. The contribution of each transport model was dependent on the applied bias; as the bias increased, the dominant conduction channel changed from the thermionic emission to PF conduction. At the same time, the hole injection barrier modulation became insensitive to the gate field, which resulted in low ON/OFF ratio in the high bias range. Since the thickness of the pentacene layer may also affect the current between the electrodes, further investigations in terms of variable thickness of the pentacene would be desirable. This research on the electrical properties of organic heterostructure based on graphene can be exploited in various organic devices, including rectifiers, LEDs, memory, and other multi-functional electrical components.

Acknowledgments

This study was achieved through support from the National Creative Research Laboratory Program (grant no. 2012026372) provided by the National Research Foundation of Korea (NRF), funded by the Korean Ministry of Science, ICT & Future Planning. G-CY and JY thank the financial

support from the Global Research Laboratory Program of the National Research Foundation of Korea (grant no. NRF-2015K1A1A2033332) and Research Institute of Advanced Materials (RIAM) of Seoul National University.

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