

# Energy Consumption Estimation of Organic Nonvolatile Memory Devices on a Flexible Plastic Substrate

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The energy consumption during the operation of organic nonvolatile memory devices fabricated on a flexible polyethylene naphthalate (PEN) substrate is investigated. For bistable resistive memory devices, the applied external voltage and time are essential factors for switching the memory cell from the OFF to ON state because the amounts of voltage and time determine the applied energy needed to set the memory cell. Using the composite material polyimide (PI) and [6,6]-phenyl-C<sub>61</sub> butyric acid methyl ester (PCBM) as the active layer of the bistable resistive memory devices on a flexible PEN substrate, nonvolatile unipolar switching behavior and good electrical reliability of PI:PCBM memory devices are observed, and the relationship between the applied energy and the switching characteristics for various applied voltages and times is characterized. The results of the performed experiments show that higher ON state currents are reached as greater set voltages or times are applied, and reliable switching behavior is observed at over  $\approx 10^{-6}$  J of applied energy with at least 4 V of applied voltage and 10 ms of pulse time.

the device cell is defined by the product of the switching voltage, current, and time. However, because the deviation of the switching time is typically larger than that of the voltage and current values in most organic memory devices, the energy consumption is particularly related to the switching speed of the devices, that is, devices with shorter switching times have lower energy consumption that much and vice versa.<sup>[20,21]</sup> With considerable research aimed at following up on superb switching properties of Si-based inorganic memory such as the switching speed of dynamic random access memory and retention times of flash memory, there have been several studies considering the factors that determine the switching time of organic memory devices.<sup>[22,23]</sup> Because the active layer of organic memory devices generally consists of an aggregated polymer blend

structure with a conducting block containing charge-trapping sites and a nonconductive host matrix, the switching process that determines the speed is highly related to morphological or conformational changes of the active layer such as phase separations, dynamic processes for the formation of metallic filaments, and isomerization, but the specific factors determining the switching speed of memory devices are still unclear.<sup>[24–28]</sup> Because the application of external energy is required to cause a morphological or conformational change of the active layer of organic memory devices, it is important to examine the quantity of applied energy needed with varying amounts of applied time and voltage bias. However, a study of energy consumption in flexible organic resistive memory devices has not previously been completed, contrary to the case of inorganic memory devices.<sup>[29,30]</sup>

Here, we examined the energy consumption for the electrical switching of organic resistive memory devices fabricated on a flexible polyethylene naphthalate (PEN) substrate. We used a composite material of polyimide (PI) and [6,6]-phenyl-C<sub>61</sub> butyric acid methyl ester (PCBM) as the active layer of our memory devices that exhibited unipolar switching behavior with reliable electrical operation in both flat and flexible configurations. To examine the energy-dependent switching behavior, we observed the statistics of the ON state currents after different set voltages and times were applied to the memory device cells in the OFF state and found that the ON state currents were linearly related to the applied energy values. Our results showed that at least  $\approx 10^{-6}$  J of applied energy per bit was needed for reliable

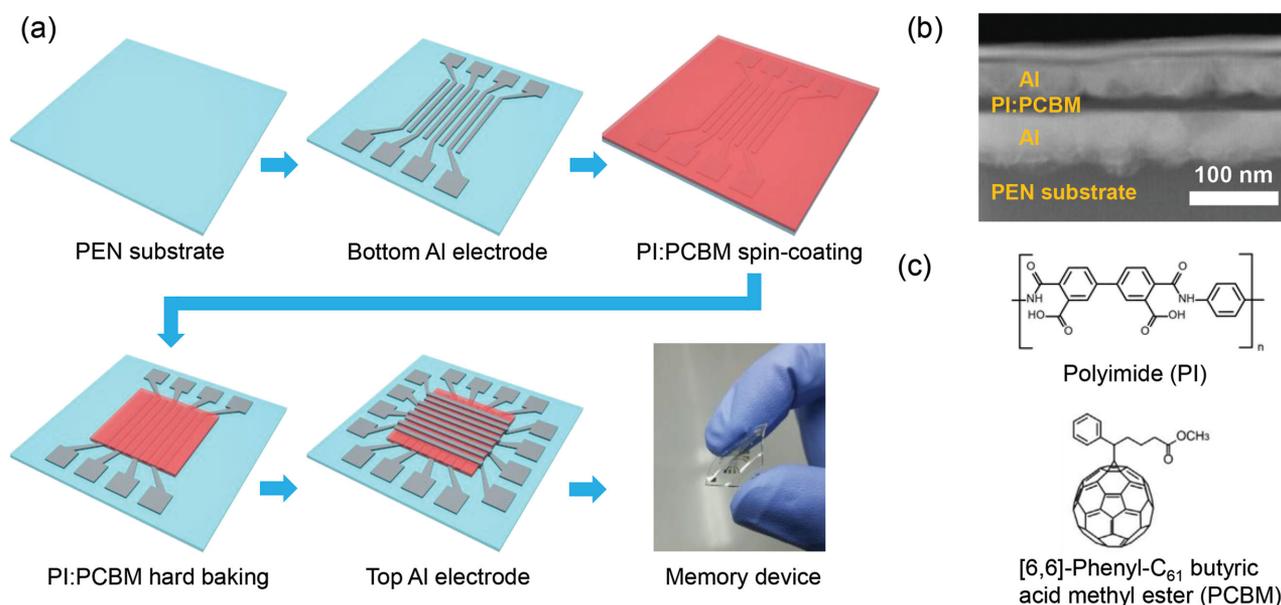
## 1. Introduction

Organic-based electronic devices, such as organic field effect transistors, solar cells, light-emitting diodes, and nonvolatile memory devices, have been intensively explored due to their potential advantages, including simple device structures, low-cost fabrication, flexibility, and low weight.<sup>[1–7]</sup> Among these, organic nonvolatile memory devices have achieved attention as a candidate for future data storage media in flexible memory devices.<sup>[8–11]</sup> Although the field of organic memory device technology has progressed, to actualize organic memory devices for practical applications, there are still several issues to solve, such as durability in the ambient environment, large-scale integration, reproducibility, uniformity of set voltages, and energy efficiency.<sup>[12–17]</sup> In particular, the energy efficiency of a device cell is very important for applying personal usage because the energy consumption of the devices is highly correlated with the cost, environment, and battery life, especially for mobile electronic products.<sup>[18,19]</sup> In general, the energy consumption of

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**Figure 1.** a) The fabrication process and an optical image of the PI:PCBM memory devices on a flexible substrate. b) Cross-sectional TEM image of a memory device. c) The molecular structure of the PI:PCBM composite material.

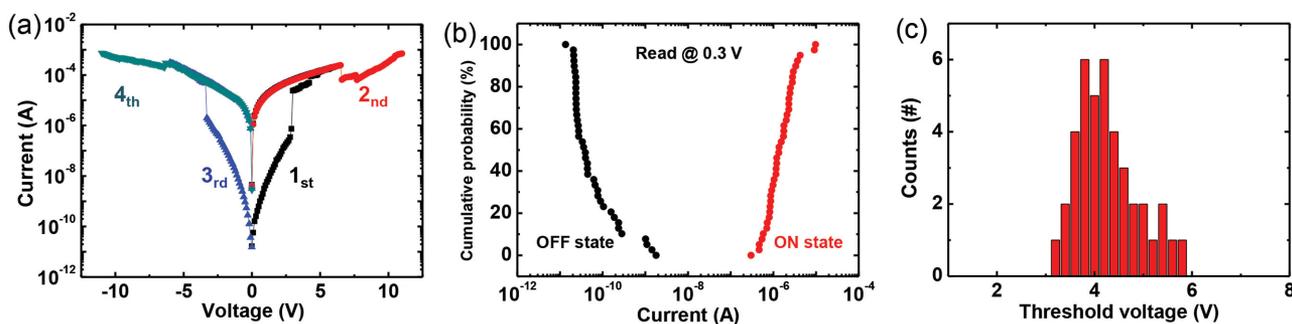
electrical switching from the OFF to ON state with a high ON current of  $\approx 10^{-6}$  A, and the scale of the set time of PI:PCBM composite memory devices was determined to be  $\approx 10$  ms.

## 2. Results and Discussion

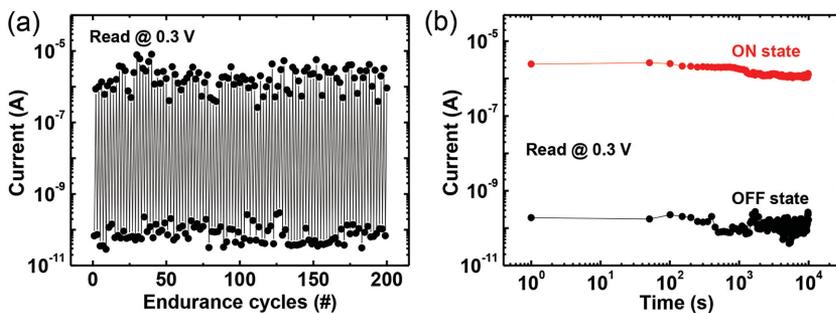
### 2.1. Memory Characteristics

Figure 1a shows the fabrication process of our PI:PCBM memory devices on a PEN substrate. The details of the device fabrication are explained in the Experimental Section. Figure 1b shows the cross-sectional TEM image of the fabricated memory devices. The vertical structure of Al/PI:PCBM/Al memory device on the PEN substrate are well separated without any Al element penetration through the PI:PCBM active layer material (Figure 1c). The detailed element profile analysis along a vertical cross section of our memory devices is shown in Figure S1 in the Supporting Information. Figure 2a shows a representative semilogarithmic current–voltage characteristic of

our PI:PCBM memory devices on a PEN substrate. To turn the device on from the initial high-resistance state (OFF state) to the low-resistance state (ON state), we applied a voltage ranging from 0 to 6 V using a dual-sweep measurement (first black line). When the applied voltage reached  $\approx 4$  V, the current level was rapidly increased by more than three orders of magnitude, indicating that the memory device switched from the OFF state to the ON state. The ON state current remained stable even when the voltage returned to 0 V, which is characteristic of nonvolatile memory devices. To turn the device off, the applied voltage was swept once from 0 to 11 V (second red line). The ON state current tracked the previous curve at low voltages and turned off above  $\approx 7$  V with a decreased state current, showing a negative differential resistance region. This unipolar repetitive switching was also observed symmetrically in the negative voltage region by a dual-sweep set process from 0 to  $-6$  V (third blue line) and a single-sweep reset process from 0 to  $-11$  V (fourth dark cyan line). These resistive switching characteristics can be explained by the charge-trapping mechanism reported by Simmons and Verderber<sup>[31]</sup> and Bozano et al.<sup>[32,33]</sup> In array-type memory



**Figure 2.** a) The representative semilogarithmic current–voltage curve, b) cumulative probability data, and c) statistical threshold voltage distribution of the PI:PCBM memory devices.



**Figure 3.** a) DC sweep endurance tests at a voltage of 0.3 V for 200 repetitive endurance cycles in the flat configuration. b) The retention tests of each resistive state for  $10^4$  s at the voltage of 0.3 V with a 50 s reading interval in the flat configuration.

devices, it is important to statistically analyze the electrical parameters of the operating cells. Figure 2b shows the cumulative probabilities of the read current of each resistive state in 40 selected operating cells of our memory devices. The ON and OFF current values indicate the measured data at a reading voltage of 0.3 V in each resistive state. The ON currents were distributed in narrow region within approximately two orders of magnitude, whereas the OFF currents appeared to be somewhat widely distributed; however, the ON and OFF state currents are separated by at least two orders of magnitude here, confirming bistability of the memory devices. Figure 2c displays the statistical distribution of the threshold voltages ( $V_{TH}$ ) of the operated memory cells. The switching process from the OFF to ON state usually occurred at  $\approx 4$  V with a narrow range of deviation, exhibiting outstanding cell-to-cell uniformity of the devices.

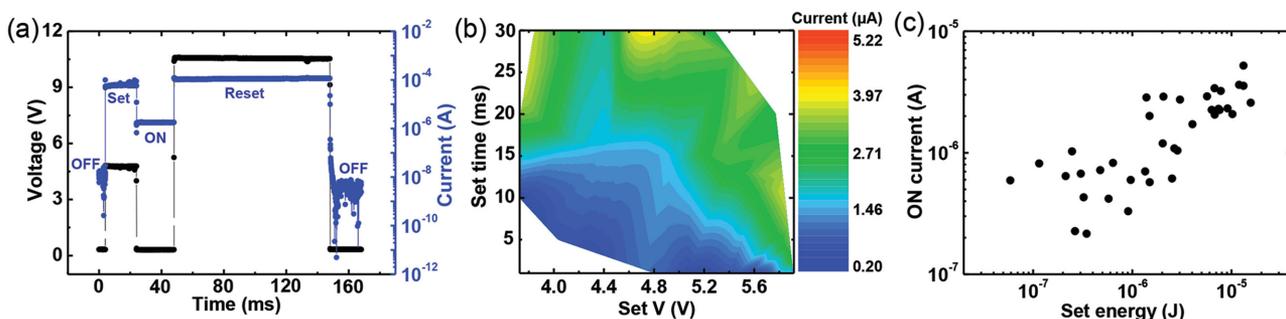
## 2.2. Endurance and Retention Characteristics

To examine the reliability of the devices under conditions of physical stress (flexing), we performed DC sweep endurance and retention tests. Figure 3a shows the measured read currents at a voltage of 0.3 V for 200 repetitive endurance cycles in the flat configuration. During the repetitive sweeps, the currents of each resistive state and the ON/OFF ratio values were well maintained without any significant electrical degradation. Figure 3b shows the read currents of each resistive state for  $10^4$  s retention times at the voltage of 0.3 V with a 50 s reading interval for the flat configuration. Similar to the endurance

tests, each resistive state current and the ON/OFF ratio values were stable, confirming the reliability of our memory devices with repetitiveness and continuity of each resistive state. The endurance and retention characteristics of the memory devices for the bent configurations (radius of 20 and 10 mm) are presented in Figure S2 in the Supporting Information.

## 2.3. Energy Consumption Analysis

To observe the simultaneous current response of the memory devices to an applied time-dependent voltage pulse, we performed pulsed current–voltage characterization tests in both the flat and bent configurations. Figure 4a shows the change of the resulting current (blue line) in response to a time-dependent voltage pulse (black line) in the flat configuration. At first, the memory cell was in the OFF state for a continuous base reading voltage of 0.3 V. After we applied a voltage pulse of 5 V for 20 ms (set process), the memory cell was switched to the ON state with a high ON current of  $\approx 10^{-6}$  A even for the low base reading voltage of 0.3 V. To switch the memory cell off, we applied a high voltage pulse of 10.5 V for 100 ms (reset process), which results in the OFF state of the memory cell with a low OFF current at the reading voltage. To examine in detail the effect of the set voltage and time on the resulting ON current of the memory cell, we performed a statistical analysis of the ON currents of the switched memory cell after applying various set voltages and times. Figure 4b shows a contour plot of the ON current versus the set voltage and time for  $\approx 40$  different data points. Naturally, when greater set voltages or times were applied, higher ON currents were reached as increased applied energy, as shown in the colored region of the plot, and the set time showed a slightly decreasing tendency as applied set voltage was increased because of the inverse relationship between set time and voltage to form the same set energy value even though the degree of that was not very high for the difference of variation range between set time and voltage. Also, at least 10 ms of set time was needed at most voltage values to stably switch on the memory cell with an ON current of  $\approx 10^{-6}$  A, which can be regarded as the minimum ON current value as shown in Figure 2b. Therefore, the scale of the set time of PI:PCBM composite memory devices is  $\approx 10$  ms.



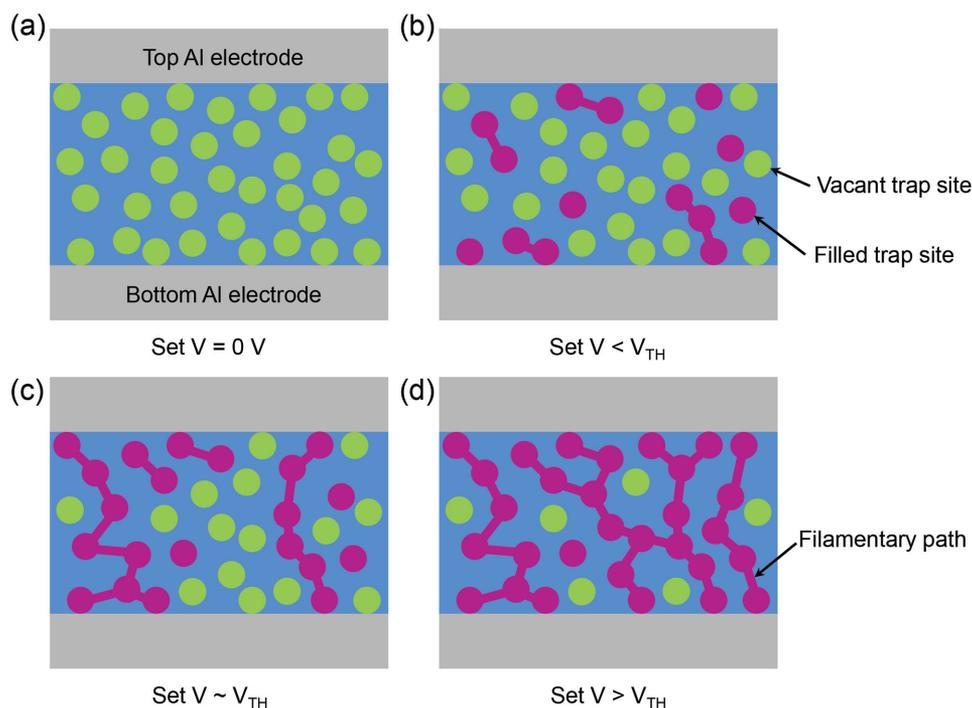
**Figure 4.** a) The current response to a time-dependent voltage pulse, b) contour plot of the ON current versus the set voltage and time, and c) the ON current versus the set energy of the memory devices in the flat configuration.

Figure 4c shows the ON current versus the set energy plot of the memory devices. Here, the equation of set energy can be simply defined as " $E$  (J) =  $V \cdot I \cdot t$  ( $V \cdot A \cdot s$ )", where the symbols inside bracket mean the dimension of variables. As expected, the result shows that as more set energy was applied, higher ON currents were obtained, and  $\approx 10^{-6}$  J of applied energy was needed to obtain reliable switching with an ON current of  $\approx 10^{-6}$  A, which showed quite high energy consumption value compared to that of the inorganic memory devices because of the structural limitation of active polymer materials with complex operating mechanism.<sup>[24,27–33]</sup> It is particularly important to figure out energy consumption value of the memory devices in this way because appropriate energy value should be applied to the memory device to show the stably repetitive endurance properties in practical device implement by avoiding misoperation from excessive or deficient injected energy based on voltage pulse. The same plots for the bent configurations (radius of 20 and 10 mm) are presented in Figure S3 (Supporting Information), and those of reset process are presented in Figure S6 in the Supporting Information.

## 2.4. Switching Mechanism Analysis

To explain the energy-dependent switching characteristics of the memory devices, we analyze the results using the charge-trapping mechanism in terms of the aggregated PI:PCBM active layer structure, as illustrated in Figure 5.<sup>[8,31–33]</sup> In common with most active layers of organic memory devices, our PI:PCBM active layer shows an aggregated polymer blend structure with randomly distributed conducting PCBM blocks

acting as charge-trapping sites throughout a nonconductive PI host matrix. When no voltage is applied, all of the trap sites in the active layer are vacant (Figure 5a). As the applied voltage is increased, a large number of charge carriers injected from the Al electrode can be captured in the near trap sites one by one, and some of the neighboring filled trap sites are able to form a current pathway through hopping conduction of charge carriers between the filled trap sites; however, they are still insufficient to form a complete carbon-rich filamentary path linking the top and bottom Al electrodes (Figure 5b). When the applied voltage reaches  $\approx V_{TH}$ , the filamentary path formation starts with a sufficiently increased number of neighboring filled trap sites, and the current level rapidly increases (see Figure 2a), exhibiting resistive switching characteristics of the memory devices from the OFF to ON state (Figure 5c). As presented in Figure S4a in the Supporting Information, the slope of the double-log plot analysis of the ON state current was calculated to be approximately 1.06 in the low voltage region (less than 1 V), indicating ohmic conduction, but it was approximately 1.29 in the high voltage region (more than 1 V), suggesting an interpretation in terms of a bulk effect with Poole–Frenkel emission.<sup>[34–36]</sup> In fact, Poole–Frenkel emission-based hopping conduction through neighboring filled-trap sites was observed as the excellent linearity of the ON state current in the  $\log(I/V)$  versus  $V^{1/2}$  plot analysis, as shown in Figure S4b in the Supporting Information.<sup>[37]</sup> Because the filamentary paths arose near the  $V_{TH}$  region, the excess energy beyond this point can be used to build other filamentary paths, so the resulting ON state currents showed a continuously increasing tendency as more energy was applied by excessive set voltage and time values (see Figure 4c). However, because the total number of trap sites is



**Figure 5.** Schematic illustrations representing the aggregated polymer blend structure of the PI:PCBM active layer at applied voltages of a) 0 V, b) less than  $V_{TH}$ , c) near  $V_{TH}$ , and d) greater than  $V_{TH}$ .

limited by the cell junction area, it is natural to encounter the saturation of filled-trap sites, filamentary paths, and switched ON state currents even in more highly applied energy (Figure 5d).<sup>[38]</sup> We observed this saturation behavior in the linear-linear plot analysis of the ON current versus the set energy (see Figure S5 in the Supporting Information). The increasing tendency of the ON current was rapid in the low set energy region ( $\approx 1 \mu\text{J}$ ), but it became remarkably indistinct in the high set energy region (more than  $\approx 5 \mu\text{J}$ ) for all device configurations, exhibiting saturation characteristics with supporting the charge-trapping mechanism to analyze the relation between the set energy and the resulting ON state currents of the memory devices.

### 3. Conclusions

In summary, we have studied the energy consumption for the electrical switching of PI:PCBM organic resistive memory devices fabricated on a flexible PEN substrate. We observed a typical unipolar switching behavior with reliable electrical operation of the memory devices, and we analyzed the energy-dependent switching characteristics by applying different set voltages and times to the memory device cells in the OFF state. Our experiments showed that at least  $\approx 10^{-6}$  J of applied energy per bit was needed for reliable electrical switching from the OFF to ON state and the scale of the set time of PI:PCBM composite memory devices was determined to be  $\approx 10$  ms. The energy-dependent switching behavior of the resulting ON state currents can be explained by a charge-trapping mechanism in the PI:PCBM active layer, supported by the linear and saturation characteristics of the ON state currents of the memory devices.

### 4. Experimental Section

**Device Fabrication:** To fabricate the organic memory devices, a flexible PEN substrate was first cleaned using a standard solvent cleaning process with acetone and isopropyl alcohol in an ultrasonic bath for 10 min, followed by a drying process in a vacuum oven at 100 °C for 3 h to evaporate the residual solvent and moisture on the PEN substrate. The bottom Al electrodes (50 nm) were deposited on the cleaned PEN substrate by a thermal evaporator using a 100  $\mu\text{m}$  line width shadow mask at a deposition rate of 0.5  $\text{\AA s}^{-1}$  and a pressure of  $\approx 10^{-6}$  Torr. To prepare the active layer for the memory devices, we used a composite material of PI:PCBM (see Figure 1c) due to its nonvolatile memory properties as well as its mechanical and electrical stability.<sup>[39,40]</sup> As a PI precursor, biphenyltetracarboxylic acid dianhydride *p*-phenylenediamine (BPDA-PPD) dissolved in *N*-methyl-2-pyrrolidone (NMP) solvent (BPDA-PPD:NMP = 1:3 weight ratio) was used. Then, a PI:PCBM composite solution was made by mixing the prepared PI solution (1 mL) and 0.5 wt% of the PCBM solution in NMP (1 mL). After a UV-ozone treatment on the bottom Al electrodes on the PEN substrate for 10 min to improve the film uniformity and device reliability,<sup>[41]</sup> the PI:PCBM solution was spin-coated onto the substrate at 1500 rpm for 35 s followed by soft-baking on a hot plate at 120 °C for 5 min in an  $\text{N}_2$ -filled glove box. For electrical probing, part of the PI:PCBM film on the pads of the bottom Al electrodes was removed by rubbing with a methanol-soaked swab followed by hard-baking at 200 °C for 60 min. The thickness of the PI:PCBM composite active film was measured to be  $\approx 20$  nm by transmission electron microscopy (TEM) analysis (see Figure 1b). Finally, the top Al electrodes (50 nm) were deposited perpendicular to the bottom Al electrodes under identical deposition conditions.

**Electrical Measurement:** A semiconductor analyzer system (Keithley 4200-SCS) with a 4200-SMU was used for the current-voltage sweep measurement and a 4225-PMU for the current response to a time-dependent voltage pulse in an  $\text{N}_2$ -filled glove box.

### Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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