Temperature Dependence of Electron Transport in ZnO Nanowire Field Effect Transistors

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***Abstract*— Nanowires (NWs) have attracted considerable interests for electronic and optoelectronic device applications. However, the carrier transport mechanisms in these NW devices have not been well understood. Here we present the electron transport of ZnO NWs field effect transistors (FETs). Our results show that the electron transport of ZnO NW FETs is governed by the space charge limited model at temperatures below a trap temperature. Above the trap temperature, the electron transport is thermionic emission dominated. Based on the space charge limited model, an accurate method is developed for field effect mobility extraction. The extracted electron carrier mobility is strongly dependent on temperature with a peak value of 51 cm^2/Vs at 167 K. Under the space-charge limited transport, the field mobility is lower in comparison with the values extracted from the thermionic emission model. The electron mobility due to space charge scattering has a value of 483 cm^2/Vs at the trap temperature with temperature dependence of $T^{4\sim5}$. The interface state density between the back gate dielectric and ZnO NWs is in the range 9.03×10^6/cm–8.72×10^7/cm at temperatures ranging from 77 to 227 K.**

***Index Terms*— Electron transport, field effect transistors (FETs), mobility, space charge limited model, ZnO nanowires (NWs).**

I. Introduction

ONE-DIMENSIONAL semiconductor materials such as single wall carbon nanotubes and semiconductor nanowires (NWs) are potential candidates for next generation electronic and optoelectronic devices [1]. However, the carrier transport in devices based on such 1-D NWs has not been well understood because of the high concentration and peculiar distribution of surface states due to their large surface-to-volume ratio [2]–[4]. Also, these semiconductor NWs are often highly defective due to their native properties and the methods they are synthesized and processed. For example, ZnO is a native n-type material and the electronic conduction in nominally undoped ZnO materials is a result from native defects such as unintentionally doped impurities (oxygen vacancies and hydrogen atoms) and structural imperfections [5]. It can be even more intangible in the case of quasi-1-D ZnO NWs devices. Owing to such complexity, the electrical transport in ZnO NW devices has so far been considered to be controversial. For example, does the electron transport of ZnO NW field effect transistors (FETs) follow the same mechanism of ZnO thin film planar FETs? Do they follow the same electron transport mechanism at different temperatures? What is the carrier mobility in ZnO NW FETs? Thus, various transport mechanisms such as thermal activation conduction [6], [7], Efros-Shklovskii variable-range-hopping (VRH) conduction [8], and Mott VRH conduction model have been proposed [9], [10]. While these models are useful to explain some experimental data, they do not provide the whole picture of electron transport in ZnO NW FETs. Most of the time, presumably ZnO NWs are considered to follow the same transport mechanism with ZnO thin films [11]. This, however, is not necessarily true because the impact of surface states needs to be seriously considered on electron transport. Thus, the low field mobility values extracted based on the conventional method for thin film planar FETs may be fundamentally inaccurate. Furthermore, just like conventional metal–oxide–semiconductor FETs, the interfacial quality between the semiconductor NWs and gate oxides is critical even dominant on the performance of NW-FETs. An effective model to extract the interfacial state density at the NWs and gate oxide interface is critically needed [12]. Therefore, it is fundamentally important to establish a model and revisit these issues. It is also critical for development of high performance NW-based devices to have good understanding of carrier transport in such devices.

In this paper, we present the electron transport mechanism of these devices. First, we propose that the electron transport is governed by the space charge limited model at temperatures below a trap temperature. Above the trap temperature, the electron transport in ZnO NW FETs is governed by thermionic emission. Second, the interfacial state density between the gate oxide and NWs are calculated. Finally, the low field mobility is extracted based on the proposed electron transport models.

II. Experiment

A. Synthesis of ZnO NW

ZnO NWs were grown using vapor-liquid-solid method as reported in [13]. Briefly, ZnO NWs were synthesized by thermally vaporizing the mixture of commercial ZnO powder

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(99%) and graphite powder (99%) with a mass ratio 1:1 in a tube furnace on a gold coated c-plane sapphire substrate. The NWs were grown at a temperature of 920 °C for 20 min in a flow of a gas mixture of 0.2% O_2/Ar with a flow rate of 50 sccm.

B. ZnO NW FETs Fabrication

For device fabrication, a 100-nm thick SiO_2 was thermally grown as the gate dielectric layer on a highly doped p-type silicon substrate, which serves as a back gate electrode. ZnO NWs were removed from the sapphire substrate after growth by sonication in ethanol and then spin-coated onto the Si substrate. Three different metal contacts (Ti/Au (30/200 nm), Al/Au (30/200 nm), and Au (230 nm) were defined by standard photolithography and deposited by electron beam evaporation to form source/drain electrodes. Like contacts on many other semiconductor NWs, all three metal contacts to ZnO NWs are Schottky-like contacts with a close Schottky barrier height due to Fermi level pinning by surface states. The distance between the source and drain Schottky contacts is around 3.2 μm. Finally, Al/Au (30/200 nm) metallization was performed after patterning and etching of gate oxide layer with buffered oxide etch solution as gate contacts.

C. I–V Characteristics of ZnO NW FETs

The fabricated devices were characterized on-wafer at room temperature and low temperatures. Room temperature measurements were performed on a Karl Suss probe station using an Agilent 4156c semiconductor device parameter analyzer. The temperature-dependent I–V measurements were performed on a cryogenic probe station (TTP4 Probe Station, Lake shore Cryotronics, Inc) from 77 to 256 K.

III. Results and Discussion

A. ZnO NW FETs Structure and DC Characteristics

Fig. 1(a) shows a 3-D schematic view of ZnO NW FETs. The ZnO NW FETs studied here have a back gate design for modulation of current flowing through NWs between source and drain Schottky contacts. Both the scanning electron micrograph and transmission electron micrograph of a fabricated ZnO NW FET are shown in Fig. 1(b). As a working device, a single NW needs to be in good contact with two electrodes. The diameter of the ZnO NWs is 100 nm. The native impurity concentration of ZnO NWs is estimated to be at the level of 10^{17}/cm^3. Fig. 1(c) and (d) shows the family I_{ds}–V_{ds} and I_{ds}–V_{gs} transfer characteristics of a typical Ti/Au contact ZnO NW FET at room temperature, respectively. From the gate modulation of the device one can observe that this is an n-channel depletion mode device with a threshold voltage around −17 V. The device exhibited an excellent current ON/OFF ratio of 10^6. Au and Al/Au contact devices also exhibited similar transfer characteristics with a similar ON/OFF current ratio.

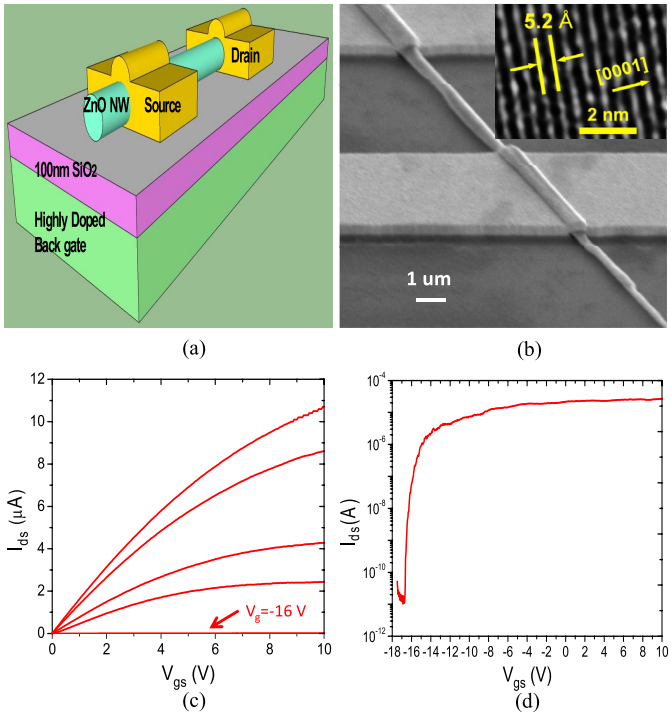

Fig. 1. (a) Schematic view of ZnO NW FETs. Schottky contacts [Ti/Au (30/200 nm), Al/Au (30/200 nm), and Au (230 nm)] are used to form source/drain electrodes. A back gate design is used to modulate the current flowing through the NW. (b) SEM image of a ZnO NW FET. The source/drain spacing is around 3.2 μm. Inset: the TEM image of an individual ZnO NW showing its lattice constant c of 5.2 Å. (c) I_{ds}–V_{ds} characteristics of a typical Ti/Au Schottky contact device. V_{ds} is from 0 to 10 V with a step of 25 mV. V_{gs} is from −16 to −8 V with a step of 2 V. (d) I_{ds}–V_{gs} transfer characteristics of a typical Ti/Au contact device. V_{gs} is from −18 to 10 V and V_{ds} is 10 V. The device is an n-channel depletion operation mode FET with a threshold voltage around −17 V.

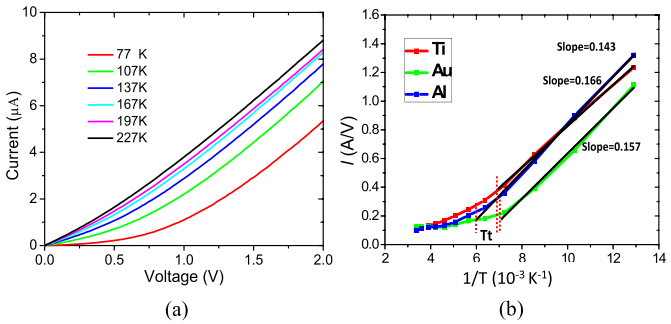

Fig. 2. (a) Temperature-dependent I–V characteristics of Ti/Au Schottky contact ZnO NW FET from 77 to 227 K when the gate terminal is floating. It shows a nonlinear I–V relationship at low temperatures. (b) I versus $1/T$ plot for Ti, Au, and Al contacted devices. The extracted slopes are 0.143 (Ti), 0.157 (Au) and 0.166 (Al), respectively. The trap temperatures (T_t) of Ti, Au and Al contacted devices are 143 K (Ti), 157 K (Au), and 166 K (Al) accordingly (as labeled in red dashed lines).

B. Electron Transport Study of ZnO NW FETs

For a better understanding of electron transport of ZnO NW FETs, temperature-dependent measurements were performed from 77 K to room temperature. During the measurements a voltage was applied between the source and drain. The gate terminal was floating. As shown in Fig. 2(a), the devices with

Ti/Au contacts exhibited a more linear I–V relationship in the high temperature range. In the low temperature range, the current and voltage shows a scaling relationship of $I \propto V^{l+1}$. This suggests that the electron transport at low temperatures is dominated by the space charge limited conduction model [14]–[17]. In this model, the exponentially distributed charge traps in a semiconductor play an important role on device I–V characteristics, resulting in the current density voltage (J–V) relationship given by

$$J \cong q^{1-l}\mu N_c \left(\frac{\varepsilon}{H}\right)^l f(l)\frac{V^{l+1}}{L^{2l+1}} \tag{1}$$

where H is the density of traps, N_c is the effective density of states in conduction band, ε is the dielectric constant of the NW, q is the electron charge, L is the electrode spacing, and μ is the carrier mobility. Here, $f(l)$ is a function of the scaling exponent $l = T_t/T$ [17]

$$f(l) = \left(\frac{l}{(l+1)}\right)^l \left(\frac{2l+1}{l+1}\right)^{l+1} \frac{1}{2^l} \tag{2}$$

where T is the measurement temperature and T_t is the trap temperature. It can be easily observed that $f(l) \approx 0.5$ if l is close to or larger than 0.55. Therefore, $f(l)$ can be viewed as a constant. T_t provides the spread of the Gaussian distribution. Due to the relationship of $I \propto V^{l+1}$, l can be extracted directly from temperature-dependent I–V characteristics [Fig. 2(a) for Ti contact devices]. Fig. 2(b) shows the plot of extracted l as a function of 1/T for Ti/Au, Au, and Al/Au contact devices. The trap temperature T_t can be determined from the slope of the curve, which gives the value in the range 143–166 K here. When $T > T_t$, trapped charges are promoted back to the conduction band by the thermal energy and the devices exhibit essentially ohmic behavior (i.e., $l+1 = 1$) with a small energy barrier; when $T < T_t$, however, space charge limited currents dominate as l increases when temperature decreases (i.e., $l+1 > 2$). This suggests that the trap density and distribution is growth condition related and independent of metal contacts to the ZnO NWs.

C. ZnO NW and SiO_2 Interface Study

Another critical issue we examined in this paper is the interfacial states between ZnO NWs and gate dielectric SiO_2 in these devices. Considering depletion takes place at ZnO NW/SiO_2 interface under a specific gate bias, this makes the structure shown in Fig. 3(a) just like a conventional MOS structure. Then, the depletion width (W_d) can be calculated as

$$\frac{qN_d}{2\varepsilon_0\varepsilon_{\mathrm{ZnO}}}W_d^2 + \frac{qN_d}{C_{\mathrm{ox}}}A + V_g - \phi_{\mathrm{ms}} = 0. \tag{3}$$

Here, N_d is the doping concentration (10^{17}/cm^3), A is the area of ZnO/SiO_2 interface given by

$$A = \frac{1}{2}R^2(\theta - \sin(\theta)) \tag{4}$$
$$(\theta = 2\cos^{-1}(1 - W_d/r)).$$

C_{ox} here is the gate-NW capacitance given by

$$C_{\mathrm{ox}} = \frac{2\pi\varepsilon_{SiO_2}\varepsilon_0 L}{\cosh^{-1}(1 + h/r)} \tag{5}$$

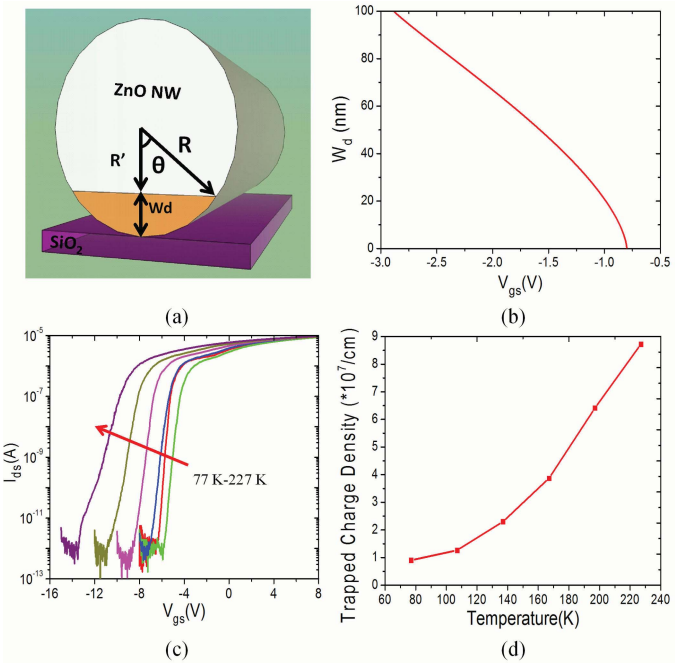

Fig. 3. (a) Schematic of depletion region at SiO_2 and ZnO NW interface. Here, W_d is the depletion width in ZnO NW, R is the physical radius of ZnO NW, and R' is the effective radius of ZnO NW, given by $(2R - W_d)/2$. W_d increases with the gate bias until the whole NW gets fully depleted. (b) Depletion width (W_d) at SiO_2/ZnO NW interface as a function of gate bias by solving (3)–(5). As shown, W_d reduces to 0 nm with a gate bias of -0.8 V and increases to 100 nm with a gate bias of -2.88 V, if no interface states are considered. (c) Temperature-dependent I_{ds}–V_{gs} transfer characteristics for Ti/Au contacted ZnO NW FETs from 77 to 227 K at $V_{\mathrm{ds}} = 2$ V. (d) Extracted trapped carrier concentration at SiO_2 and ZnO NW interface for Ti/Au contacted ZnO NW FETs. The trap charge density increases from 9.03×10^6/cm to 8.72×10^7/cm with the temperature increasing from 77 to 227 K.

where L is the source drain spacing, h is the thickness of SiO_2, and r is the physical radius of NWs. By solving (3) through (5), we can get depletion width as a function of gate bias [Fig. 3(b)]. The result shows that at a gate bias of -2.88 V, the NW is fully depleted, or W_d reaches the diameter of NW. Also the flat-band voltage appears at -0.8 V. Thus, -2.88 V is the theoretical gate threshold voltage, if no interfacial states are considered. However, the experimental gate threshold voltage is always more negative [Fig. 3(c)], which is a strong evidence for the existence of trapped charge at the ZnO NW/SiO_2 interface. In this case, the interface charge density is given by the product of C_{ox} and the difference between the theoretical and actual gate threshold voltage [shown in Fig. 3(d)]. As one can observe, these trapped charge density at the NW and gate oxide interface increases from 9.03×10^6/cm to 8.72×10^7/cm with the temperature increasing from 77 to 227 K, due to the fact that more ionized donor states at a higher thermal energy result in a higher carrier concentration in the channel.

D. Field Mobility Extraction of ZnO NW FETs.

Based on space-charge-limited current model in [17], the current density in thin wires depends on both the applied voltage and NW dimension (R/L ratio), which is defined as

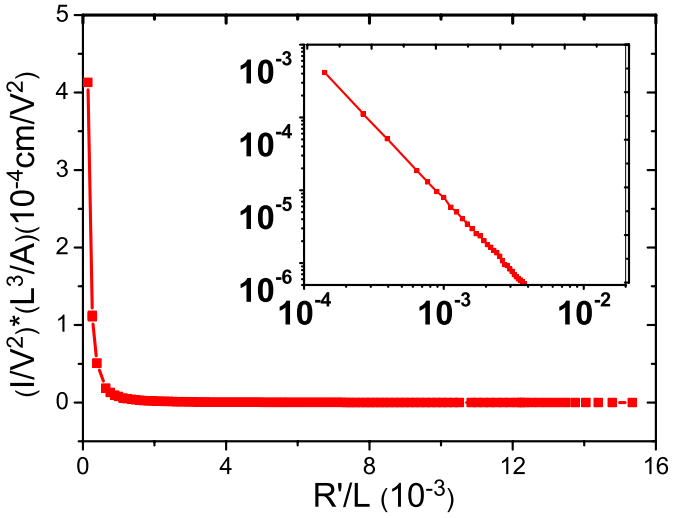

Fig. 4. Scaling behavior for Ti/Au contacted ZnO NW FETs with gate biases ranging from −5 to 0.8 V at 77 K. The inset is the same data plotted on a log-log scale with a slope close to −2. The plots show $(IL^3)/(AV^2)$ follows the scaling relationship $\xi_0(R'/L)^{-2}$ well.

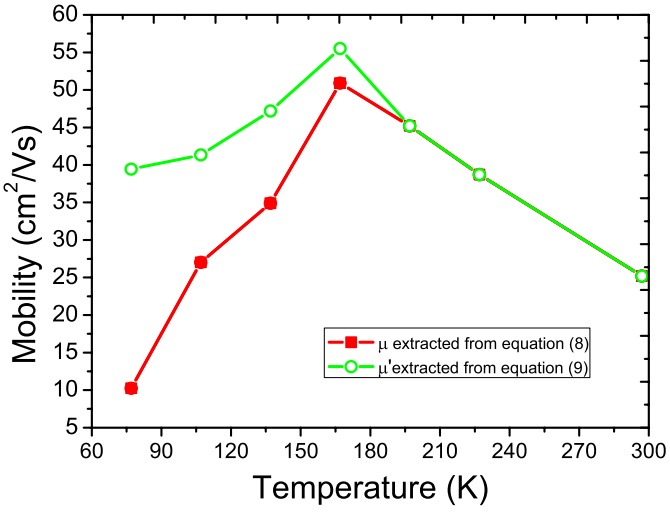

Fig. 5. Extracted carrier mobility in low field region as a function of temperature. The mobility values below 167 K are extracted using (8) (red line) and (9) (green line), respectively. The mobility values above 167 K are all extracted from (9).

$\zeta\ (R/L)$ here

$$J = \xi(R/L)\frac{\varepsilon\mu}{L^3}V^2 \tag{6}$$

where ε is dielectric contestant of ZnO material, μ is carrier field mobility, and V is the drain to source voltage. Since the depletion happens at the ZnO/SiO_2 interface, R here should be replaced by the effective radius R', which is the radius of non-depletion region given by $(2R - W_d)/2$. Thus, the actual R'/L varies from 0 to 0.0156 with the gate bias varying from −2.88 to −0.8 V. It is well known that one signature for space charge limited model is the existence of crossover voltage V_c in the log-log plot of I–V characteristics [15]. However, no such crossover voltages were observed on ZnO NW FETs based on our temperature-dependent measurements. Talin *et al.* [17] already demonstrated that the crossover voltage in another widebandgap semiconductor GaN NW material is scaled by $1/\xi(R/L)$ compared to the bulk material case. Indeed, when R'/L is small enough, we have a good approximation that

$$\xi(R'/L) \approx \xi_0(R'/L)^{-2} \tag{7}$$

where ξ_0 has a constant value close to 1 [17]. Thus, we have $Vc \sim (R'/L)^2 Vc^{\text{bulk}}$ and the crossover voltage is at least eight orders smaller than that of FETs on a normal ZnO bulk material (typically around 10 V) [18], leading to a value less than one micro-volt. Thus, no crossover voltage was observed in this paper.

Although the physical radius of ZnO NW is fixed at 50 nm, the effective radius R' varies as a function of gate bias. Fig. 4 shows a plot of IL^3/AV^2 as a function of R'/L, which follows the scaling relationship $\xi_0(R'/L)^{-2}$ very well. In the inset of Fig. 4, the log scale plot of IL^3/AV^2 versus log (R'/L) clearly shows a slope of −2, which confirms that the current flowing through the ZnO NW indeed follows the space-charge-limited model. If we rewrite (6) in log scale as

$$\log_{10}\left(\frac{IL^3}{AV^2}\right) = -2\log_{10}(R'/L) + \log_{10}(\varepsilon\xi_0\mu) \tag{8}$$

then the low field electron mobility (μ) in these ZnO NW FETs can be extracted from the intercept of the log plot. Based on the temperature-dependent I_{ds}–V_{gs} transfer characteristics, the extracted field mobility as a function of temperature is shown in Fig. 5. Starting from 77 K, the mobility increases upon heating until it reaches the maximum value of 51 cm^2/Vs at 167 K, which is very close to the trap temperature we extracted above (shown in Fig. 5 red line) This is likely due to that the scattering between electrons and space charges is dominant as a result of the electron hoping process and the slow motion of electrons at low temperatures. Above the trap temperature, however, electron transport mechanism is no longer space charge dominant and the electron space charge scattering gets negligible. Thus, instead of using (8), the following equation is used for extraction of field mobility at high temperatures [11]:

$$\mu' = \frac{dI_{ds}}{dV_g}\frac{L^2}{V_{ds}C} \tag{9}$$

where L is the NW channel length (~3.2 μm), C is the gate-NW capacitance given by (5) and $V_{ds} = 2$ V. The results show a clear mobility decreasing upon heating in this region, giving mobility values of 45.2, 38.7, and 25.2 cm^2/Vs at 197 K, 227 K and room temperature, respectively. This is likely because above the trap temperature the mobility is more dominated by phonon scattering as temperature increases. For comparison, the mobility values (μ') below the trap temperature extracted using (9) are also shown in Fig. 5. Clearly, the conventional method for thin film planar FETs [e.g., (9)] overestimates the low carrier mobility and results in relatively higher values below the trap temperature. If the carrier mobility due to space

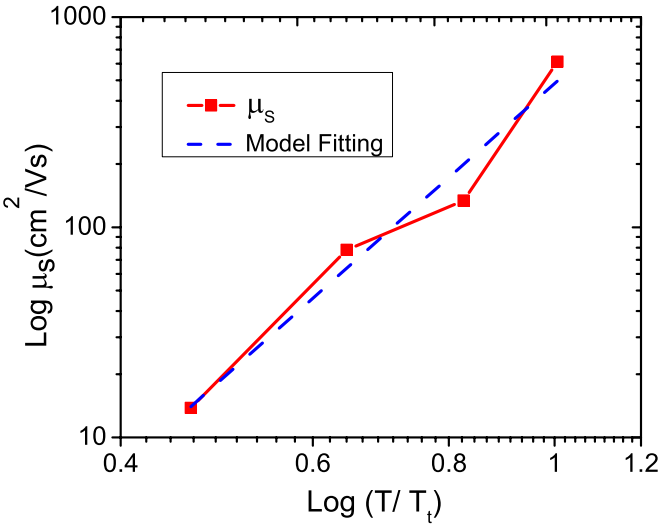

Fig. 6. Electron mobility due to space charge scattering μ_s as a function of normalized temperature in log-log scale (red line). Model fitting with (11) (blue dashed line).

charge scattering is μ_s, we have

$$\frac{1}{\mu} = \frac{1}{\mu'} + \frac{1}{\mu_s}. \tag{10}$$

Fig. 6 shows the values of μ_s as a function of temperature below the trap temperature. If we hypothesize that the space charge scattering rate is proportional to T^{-n}, we can propose the following model:

$$\mu_s = \mu_{s\_t} \left(\frac{T}{T_t}\right)^n \tag{11}$$

where μ_{s_t} is the electron mobility due to space charge scattering at the trap temperature and n is the exponent to be decided in the model. By fitting the values to (11) below, we obtain the μ_{s_t} of 483 cm^2/Vs and the exponent n value of ~4.6, or in the range 4 ~ 5. Our results presented here reveal that NW-based field effect devices, due to the unique geometric characteristics, may exhibit different electron transport properties at different bias and temperature conditions. Specifically traps like oxygen vacancies and surface and interface states play a critical role on the carrier transport and device performance. Though the model and method developed here are based on ZnO NW FETs, it is worthy to point out that the approach presented here is applicable to other 1-D semiconductor NW FETs such as carbon nanotubes, Si, Ge, and GaN NWs. The approach developed here can be a powerful method to study the effects of surface and interface traps and charges and surface passivation on field effect mobility in NW FET devices.

IV. Conclusion

In summary, the temperature-dependent I–V measurements reveal that the transport mechanism in ZnO NW FETs is temperature dependent and surface states related. At low temperatures (77–167 K), the current is dominated by exponentially distributed charge traps on ZnO surface and exhibits scaling relationship of $I \propto V^{l+1}$. The dimension scaling properties of I–V characteristics further confirm the strong space charge limited current at low temperatures in ZnO NWs. The ZnO NW FETs have a peak carrier mobility of 51 cm^2/Vs at the trap temperature (167 K). The electron mobility due to space charge scattering has a $T^{4\sim5}$ dependence with a value of 483 cm^2/Vs at the trap temperature. The interface state density between ZnO NWs and back gate dielectric is in the range 9.03 × 10^6/cm–8.72 × 10^7/cm at temperatures ranging from 77 to 227 K. The approach developed in this paper can be a versatile platform for transport study of semiconductor NW FETs.

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