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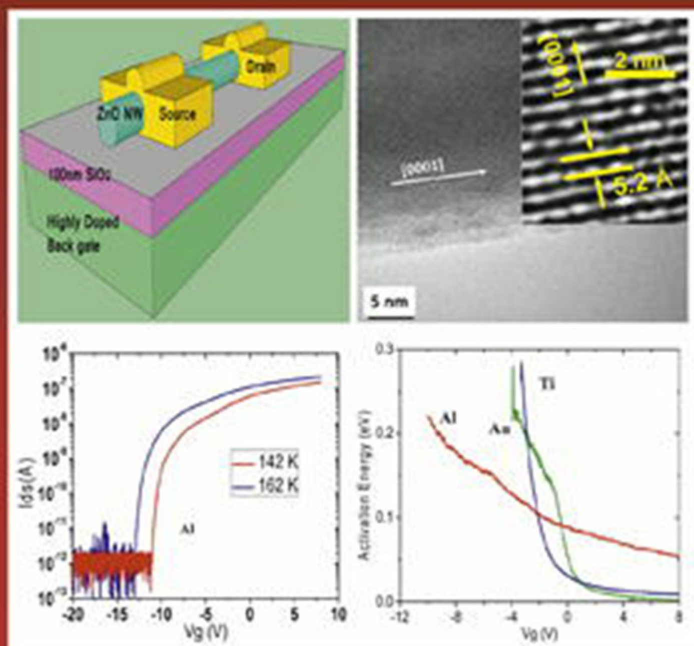

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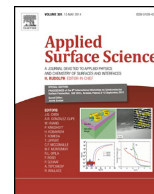

Analysis of surface states in ZnO nanowire field effect transistors

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ABSTRACT

Nanowires (NWs) have attracted considerable interests for scaled electronic and optoelectronic device applications. However, NW based semiconductor devices normally suffer from surface states due to the existence of dangling bonds or surface reconstruction. Because of their large surface-to-volume ratio, surface states in NWs can easily affect the metallic contacts to NWs and electron transport in NW. Here, we present ZnO NW surface analysis by performing current–voltage characterization on ZnO NW Schottky barrier field effect transistors with different metal contacts (Ti, Al, Au) at both room temperature and cryogenic temperature. Our results show that three metal contacts are all Schottky contacts to ZnO NWs due to surface states. Our further study reveals: (a) the surface states related Schottky barrier height (SBH) can be extracted from a back to back Schottky diodes model and the SBH values are in the range of 0.34–0.37 eV for three metal contacts; (b) the trap activation energy determined from the Arrhenius plots of different Schottky metal contacts is in the range of 0.23–0.29 eV, which is oxygen vacancies related; and (c) based on the space-charge-limited model, the surface state density of ZnO NW is in the range of 1.04×10^{10}–1.24×10^{10}/cm^2.

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1. Introduction

One-dimensional semiconductor materials such as single wall carbon nanotubes and semiconductor nanowires (NW) are promising candidates for nanoscale electronic and optoelectronic devices [1]. However, a major issue of 1-D NW semiconductor materials is from the surface states. This is because NWs, synthesized either by bottom-up or top-down technique, are often highly-defective due to the existence of dangling bonds or surface reconstruction [2–4]. The disordered nature of NW surface makes metal to semiconductor NW contacts exhibit vastly different, from linear ohmic to rectifying Schottky. This is because the NW surface states can produce randomly localized charges, which causes Fermi-level pinning [5,6]. Therefore, the properties of metal to semiconductor NW contacts are strongly dependent on interfacial properties. Even using the same metallic contacts, the current–voltage (*I*–*V*) characteristics of NW devices are generally different from thin film devices. In addition, the carrier transport in semiconductor NWs is largely impacted by the disordered potentials [7]. As a result, the conductivity or carrier mobility in these semiconductor NWs can be very sensitive to the surface states. Under some extreme conditions (e.g. low temperature), the electron transport mechanism in semiconductor NWs can even change from thermally activated conduction to other activated conduction such as surface states induced space charge hopping [8,9]. Thus, NW surface analysis is essential for understanding the electron transport mechanism and improving device performance. Usually, *C*–*V* measurement (e.g. deep-level-transient-spectroscopy) is the first choice for both qualitative and quantitative analysis of interface states and defects in bulk material [10]. However, it becomes more challenging to directly measure the capacitance of individual semiconductor NWs because of the ultra-small capacitances intrinsic to NW (aF to fF level) over large background parasitic capacitances (pF level) [11]. Thus, *I*–*V* characterization of NW based electrical devices remains a practical method for NW surface analysis.

In this study, we present ZnO NW surface analysis by performing *I*–*V* characterization on ZnO NW Schottky barrier field effect transistors (SB-FETs) at both room temperature and cryogenic temperature. ZnO is a native n-type semiconductor material and the electronic conduction in nominally un-doped ZnO materials (NWs or thin films) is a result from native defects such as unintentionally doped impurities (oxygen vacancies and hydrogen atoms) and structural imperfections [12]. Because of the lacking of an established model, the hypothesis is that metal contacts on ZnO NWs exhibit the same or similar characteristics with those contacts on ZnO thin films

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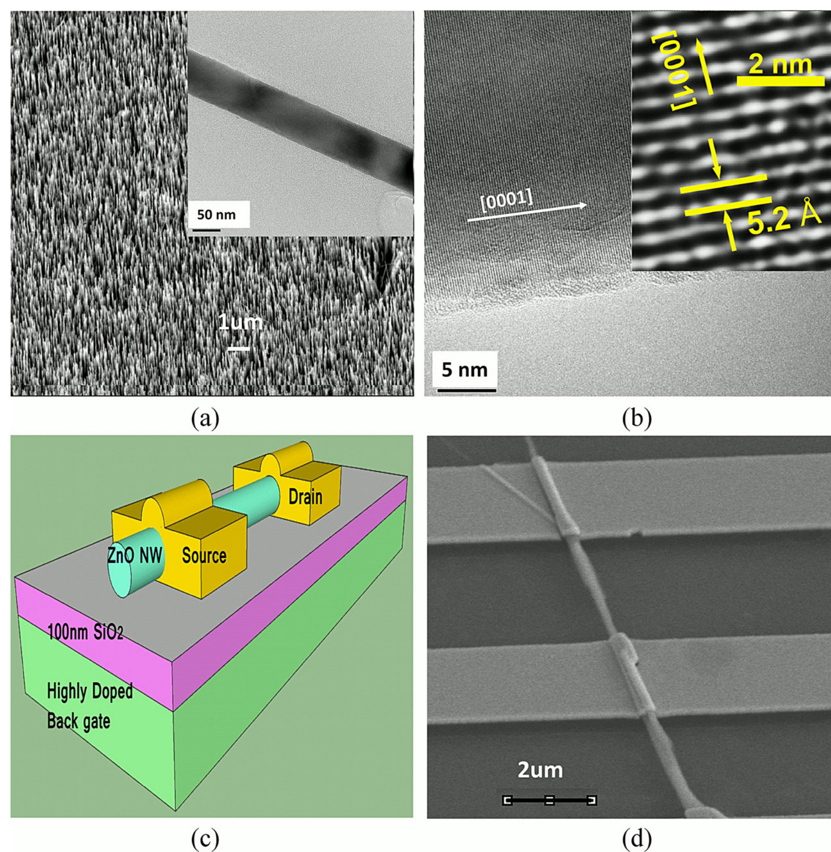

Fig. 1. (a) SEM image of ZnO NWs grown on gold coated sapphire substrate by thermally vaporizing of commercial ZnO powder and graphite powder. Inset is the TEM image of an individual ZnO NW showing its diameter is around 100 nm. (b) TEM image of an individual ZnO NW showing its [0 0 0 1] preferred growth direction. Inset is the zoom-in TEM image of an individual ZnO NW showing its lattice constant *c* of 5.2 Å. (c) Schematic view of ZnO NW FETs. Schottky contacts (Ti/Au(30/200 nm), Al/Au(30/200 nm), and Au (230 nm)) are used to form source/drain electrodes. A back gate design is used to modulate the current flowing through the NW. (d) SEM image of ZnO NWs FET, the source/drain spacing is around 3.2 μm.

[13]. This, however, is not necessarily true due to the high surface to volume ratio of NWs, hence the Fermi-level can be pinned by surface states, something more commonly observed in metal contacts to semiconductor NWs with a small energy bandgap [5]. In this paper, a back-to-back Schottky diodes model is applied to extract Schottky barrier height between metal contacts and ZnO NWs. Also, both activation energy and density of ZnO NW surface states are quantitative analyzed by temperature dependent *I–V* characterization.

2. Experimental

2.1. Synthesis of ZnO NW

ZnO NWs were grown using vapor–liquid–solid method as reported previously [14]. Briefly, ZnO NWs were synthesized by thermally vaporizing the mixture of commercial ZnO powder (99%) and graphite powder (99%) with a mass ratio 1:1 in a tube furnace on a gold coated *c*-plane sapphire substrate. The NWs were grown at a temperature of 920 °C for 20 min in a flow of a gas mixture of 0.2% O_2/Ar with a flow rate of 50 sccm.

2.2. ZnO NW FETs fabrication

For device fabrication, a 100 nm thick SiO_2 was thermally-grown as the gate dielectric layer on a highly doped p-type silicon substrate, which serves as a back gate electrode. ZnO NWs were removed from the sapphire substrate after growth by sonication in ethanol and then spin-coated onto the Si substrate. Three different Schottky contacts (Ti/Au (30/200 nm), Al/Au (30/200 nm), and Au (230 nm) were defined by standard photolithography and deposited by electron beam evaporation to form source/drain electrodes. The distance between the source and drain contacts is around 3.2 μm. Al/Au (30/200 nm) metallization was performed after patterning and etching of gate oxide layer as gate contacts.

2.3. I–V characteristics of ZnO NW FETs

Room temperature measurements were performed on a Karl Suss probe station using an Agilent 4156c semiconductor device parameter analyzer. The temperature dependent *I–V* measurements were performed on a cryogenic probe station (TTP4 Probe Station, Lake shore Cryotronics, Inc.) from 77 to 256 K.

3. Results and discussion

3.1. Morphology of ZnO NW and ZnO NW FETs structure

Fig. 1(a) shows the scanning electron microscope (SEM) image of vertically and uniformly grown ZnO NWs on the entire gold coated sapphire substrate. The high resolution transmission electron microscope (HRTEM) image of grown ZnO NWs is shown in Fig. 1(b). Clearly, [0 0 0 1] is the preferred growth direction. The diameter of the ZnO NWs is about 100 nm. The ZnO NW FETs studied here have a back gate design for modulation of current flowing through NWs between source and drain contacts. Fig. 1(c) shows a schematic view of ZnO NW FETs. The micrograph of a fabricated ZnO NW FET is shown in Fig. 1(d).

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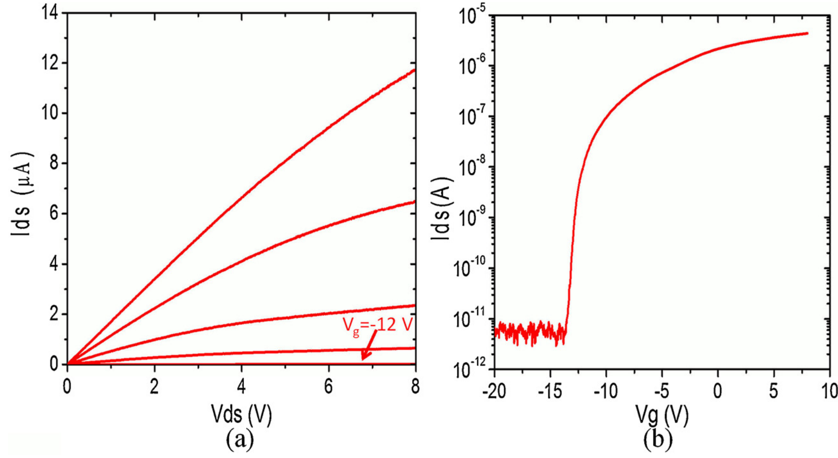

Fig. 2. (a) V_{ds}–I_{ds} characteristics of a typical Al/Au contact device. V_{ds} is from 0 V to 8 V with a step of 25 mV and V_{gs} is from −12 V to 4 V with a step of 4 V. (b) V_g–I_{ds} transfer characteristics of a typical Al/Au contact device. The device is an n-channel depletion operation mode with a threshold voltage around −13 V at V_{ds} of 2 V.

3.2. Room temperature I–V characterization and modeling

The fabricated devices were characterized on-wafer in air at room temperature first. It is common to observe performance variation between single NW FETs, due to slight impurity density and diameter difference in these CVD grown ZnO NWs. For extensive measurement and data analysis, only devices that can be fully pinched-off and sustain for repeated voltage scans were picked. Fig. 2(a) and (b) shows the family of I_{ds}–V_{ds} and I_{ds}–V_{gs} transfer characteristics of a typical Al/Au contact ZnO NW FET at room temperature, respectively. From the gate modulation of the device one can see that this is an n-channel depletion mode device with a threshold voltage around −13 V. The device exhibited an excellent current on/off ratio of more than 10^6. Au and Ti/Au contact devices also exhibited similar transfer characteristics with a similar on/off current ratio (see later in Fig. 6).

The native impurity concentration of ZnO NWs is estimated to be at the level of $5 \times 10^{17}/\text{cm}^3$ with the following equation [15]

$$n_e = \frac{V_{th}C}{q\pi r^2 L} \quad (1)$$

where V_{th} is the gate threshold voltage, r is the ZnO NW radius, L is the source to drain spacing 3.2 μm. Here C is the back gate to NW capacitance given by [14],

$$C = \frac{2\pi\epsilon_0\epsilon_{SiO_2}L}{\cos^{-1}(1 + h/r)} \quad (2)$$

where h is the thickness of SiO_2, ε_0 is the dielectric constant of vacuum, ϵ_{SiO_2} is the effective dielectric constant of SiO_2 (1.95) [16]. Since V_{th} varies between devices, the average value of −11 V here is used.

The work function of ZnO NWs is ∼4.5 eV at the concentration of $5 \times 10^{17}/\text{cm}^3$ [17]. If we assume no surface states take place, the theoretical energy barrier height for Au, Al/Au and Ti/Au contact would be 0.74 eV, −0.38 eV, and −0.21 eV, respectively [18]. In other words, Al and Ti should form ohmic contacts on these ZnO NWs and Au should form Schottky barrier contacts. Indeed it has been assumed that low work function metals such as Ti would form ohmic contacts on ZnO NWs [19]. However, according to room temperature source to drain two terminal measurement results with gate terminal floating (shown in Fig. 3), none of metal contacts show a perfect linear I–V relationship across 0 V. In fact, in all cases Schottky like contacts rather than ohmic contacts are formed in the source and drain regions of these devices. It is also worthy to note that these devices are different from a regular Schottky diode for: (a) It is hard to find the diode turn on voltage; (b) I–V curve is symmetrical in forward and reverse bias regions instead of rectify behavior; and (c) I–V shows reasonable linearity in high bias region (from 3 V to 5 V). Thus, a conventional thermionic emission model cannot be simply applied here.

To address this issue, we model our ZnO NW based FETs as a pair of back to back Schottky diodes in parallel with a shunt conductor as shown in Fig. 4(a). In this model, the symmetrical Schottky barriers between metal contacts and ZnO NW at two sides are presented by a pair of back to back Schottky diodes. Once the lateral voltage drop V_s is established at either side, the current will flow as like in a reversely-biased metal-n-ZnO Schottky diode. Also, considering the extremely small cross section and depletion width of ZnO NW, few volts bias can actually cause a huge effective electrical field (in 10^6 V/cm range). Thus, the effects such as image force lowing given by [20]

$$\Delta\phi_B = \left(\frac{q^3 N|\psi_s|}{8\pi^2\epsilon_s^3}\right)^{1/4} \quad (3)$$

and electron tunneling cannot be ignored. Here, N is the doping centration of ZnO NW; ε_s is dielectric constant (8.5) of ZnO material; ψ_s is surface potential given by

$$|\psi_s| = \phi_{Bn0} - \phi_n + V_R \quad (4)$$

where ϕ_{Bn0} is initial barrier height without image force lowing, ϕ_n is Fermi level to conduction band difference in bulk ZnO material, V_R

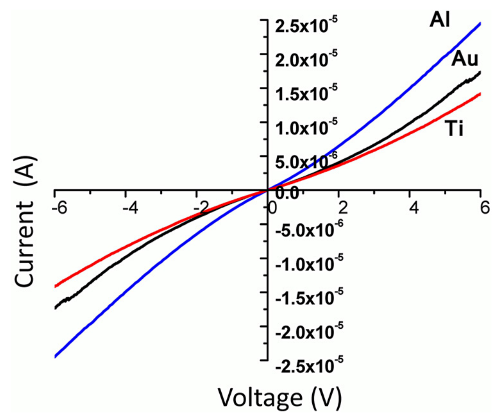

Fig. 3. Room temperature I–V characterize of ZnO NW SB-FETs with different metal contacts. During measurements a voltage was applied between source and drain. The gate terminal was floating.

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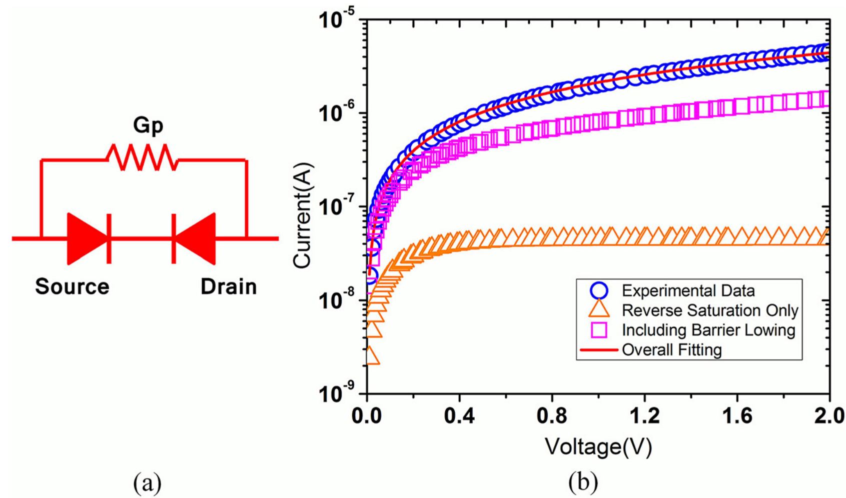

Fig. 4. (a) Circuit model used for room temperature I–V modeling. A pair of back to back diodes is used to present Schottky contacts between ZnO NW and source/drain metal. A shunt conductance G_p is used to present a parallel current path due to barrier lowing effect and tunneling effect under bias. (b) Comparison modeling data with two terminal measurement data of a Ti/Au contact ZnO NW SB-FETs: modeling data including reverse saturation current only (solid yellow line); modeling data including barrier lowing effect (pink solid line); modeling data including shunt conductance G_p (solid red line); experimental data (blue dot line). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

is the applied bias. Since ϕ_{Bn0} and ϕ_n are theoretically constant values for a given metal contact, ψ_s is a function of applied bias. When the bias goes up, the Schottky barrier height decreases due to the image force lowering effect, which causes a higher tunneling current. Therefore, a shunt conductance G_p is applied here to present a parallel tunneling current path. In this model, the reversely-biased Schottky barrier only dominates in the low bias range and G_p current path dominates the overall current level in the high bias range. This explains both I–V nonlinearity in low bias range and good linearity from 3 V to 5 V. Fig. 4(b) shows the fitting results based on the model. Based on this modeling strategy, the fitting is performed in a two-step process. Firstly, I–V data between 0.01 V and 0.1 V are chosen for reversely-biased Schottky current fitting with the following equation:

$$I = A_{eff}A^*T^2 \exp\left(-q\frac{\phi_{Bn0} - \Delta\phi_B}{kT}\right)\left(1 - \exp\left(-q\frac{V_R}{nkT}\right)\right) \qquad (5)$$

Here A_{eff} is roughly the surface area of a 100 nm-thick, 2 μm-long cylinder (Schottky contact area), A^* (=32 cm^{-2} K^{-2} A) is Richardson's constant [21], n is the ideal factor of the diode, k is the Boltzmann's constant, T is the temperature in Kelvin and $\Delta\phi_B$ is given by Eqs. (3) and (4). Thus, the value of initial barrier height and ideal factor can be extracted first without knowing G_p. By substituting the extracted ϕ_{Bn0} of 0.34 eV and ideal factor of 6 value back into Eq. (5), we can get yellow curve (reverse saturation current only) and pink curve (reverse saturation current including barrier lowing effect) in Fig. 4(b). It is clear that reversely-biased Schottky current model agrees with experimental data (blue dots curve in Fig. 4(b)) well in low bias range. Secondly, the shunt conductance G_p is added to achieve overall I–V fitting (solid red curve in Fig. 4(b)) by adding

$$I = G_p * V_R \qquad (6)$$

term to Eq. (5). Here extracted G_p is 1.75 × 10^{-6} S and fitting data agrees with experimental data well in the whole bias range. Similarly, the parameters of ϕ_{Bn0}, n and G_p for Al/Au and Au contact ZnO NW devices are also extracted based on the same model and listed in Table 1, respectively. The extracted ϕ_{Bn0} values of these three Schottky contacts are all in the range of 0.34–0.37 eV, which is very close to oxygen vacancy energy level reported in ZnO films [10,22,23]. The relative invariance of extracted Schottky barrier height from metal work functions suggests that Fermi level is partially pinned by oxygen vacancies on the NW surface and metal contacts to ZnO NWs are governed by the Bardeen model. With the above model, one can extract device parameters (e.g. Schottky barrier height) without having a good ohmic contact at one side of NW. Indeed, to have a good ohmic contact on semiconductor NWs is always challenging.

Table 1
Extracted parameters for Ti/Au, Al/Au and Au contacted ZnO SB-FETs.

	Ti/Au	Al/Au	Au
Barrier height ϕ_{Bn0} (eV)	0.34	0.35	0.37
Ideal factor n	7	6.2	5.6
Shunt conductance G_p (μS)	0.8	1.2	1.7
Trap temperature (K)	143	157	166

In the above model, an assumption we made is that the series resistance or the NW resistance is negligible compared with the shunt resistance or the contact resistance. To confirm this assumption, we measured the contact and NW resistances on a device crossing three contact pads. The circuits under 2-probe and 3-probe measurements are shown in the inset of Fig. 5. The contact resistance (R_c) is determined by

$$R_c = R_{2\text{probe}} - R_{3\text{probe}} = (2R_c + R_{nw}) - (R_c + R_{nw}) \qquad (7)$$

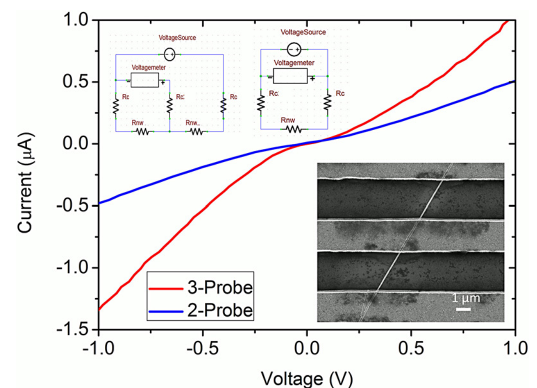

Fig. 5. I–V characteristics of a device by 2-probe and 3-probe measurements. Insets: SEM micrograph of the device and circuit models of 2-probe and 3-probe measurements.

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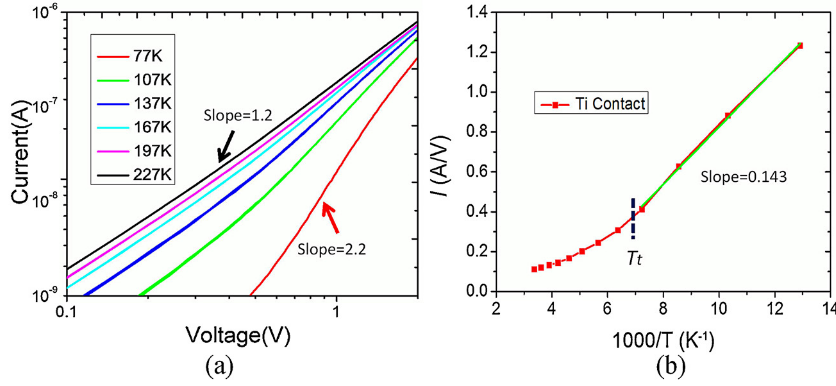

Fig. 6. (a) Plot of temperature dependent *I–V* characteristics of Ti/Au contact ZnO NW SB from 77 K to 227 K when the gate terminal is floating in log-log scale. It shows a nonlinear *I–V* relationship at low temperatures. (b) *l* versus *1/T* plot for Ti/Au contacts. The extracted slope is 0.143 and the trap temperature (T_t) of Ti is 143 K accordingly (as labeled in blue dash lines). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

where R_{2probe} and R_{3probe} are the resistances measured by 2-probe and 3-probe methods, respectively. The measured R_{2probe} (1.85 MΩ) is about two times of R_{3probe} (0.86 MΩ), indicating the NW resistance is negligible compared with the contact resistance. The measured contact resistance is about 1 MΩ, which is actually very close to the extracted shunt resistance based on the above model.

3.3. *Cryogenic I–V characterization*

3.3.1. *Trap temperature extraction*

In order to quantitatively decide the activation energy and density of ZnO NW surface states, the temperature dependent *I–V* characteristics of different Schottky contact devices were performed from 77 K to room temperature. During the measurements a voltage was applied between source and drain. The gate terminal was floating. As shown in Fig. 6(a), the devices with Ti/Au contacts exhibited a close to linear *I–V* relationship with $I \propto V^{1.2}$ at the high temperature range. In the low temperature range, the current and voltage shows a scaling relationship of $I \propto V^{l+1}$. This suggests that the electron transport at low temperatures is dominated by the space charge limited conduction model [24–27]. In this model, the exponentially distributed charge traps in a semiconductor play an important role on device *I–V* characteristics, resulting in the current density voltage (*J–V*) relationship given by

$$J \cong q^{1-l}\mu N_c \left(\frac{\epsilon}{H}\right)^l f(l)\frac{V^{l+1}}{L^{2l+1}} \quad (8)$$

where *H* is the density of traps, N_c is the effective density of states in conduction band, ε is the dielectric constant of the nanowire, *q* is the electron charge, *L* is the electrode spacing, and μ is the carrier mobility. Here *f*(*l*) is a function of the scaling exponent $l = T_t/T$,

$$f(l) = \left(\frac{l}{(l+1)}\right)^l \left(\frac{2l+1}{l+1}\right)^{l+1} \frac{1}{2^l} \quad (9)$$

where *T* is the measurement temperature and T_t is the trap temperature. It can be easily seen that $f(l) \approx 0.5$ for *l* close to 0.55. Therefore, *f*(*l*) can be viewed as a constant. T_t provides the spread of the Gaussian distribution. Due to the relationship of $I \propto V^{l+1}$, *l* can be extracted directly from temperature dependent *I–V* characteristics (see Fig. 6(a) for Ti/Au contact devices). Fig. 6(b) shows the plot of extracted *l* as a function of *1/T* for Ti/Au contact devices. The trap temperature T_t can be determined from the slope of the curve, which gives the value of 143 K here. The trap temperatures of Al/Au and Au contact devices are extracted in a similar way and listed in Table 1. When $T > T_t$, trapped charges are promoted back to the conduction band by the thermal energy and the devices exhibit Schottky behavior (i.e., $l + 1 \approx 1$). The extracted Schottky barrier height is 0.3 eV based on the *I–V* curve at 256 K. This value is close to the value at room temperature. When $T < T_t$, however, space charge limited currents dominate as *l* increases when temperature decreases (i.e., $l + 1 > 2$). This suggests that the trap density and distribution is growth condition related and independent of metal contacts to the ZnO NWs.

3.3.2. *Activation energy extraction*

In order to decide the activation energy of ZnO NW surface states, the temperature dependent I_{ds}–V_{gs} characteristics of different Schottky contact devices were measured in a temperature range close to T_t (142–162 K) at different gate biases (shown in Fig. 7(a)–(c)). Based on the Arrhenius plot of log(I_d) versus 1000/*T* at different gate biases (Fig. 7(d)–(f)) [28], the activation energy can be extracted by performing a linear fitting at every gate bias above threshold voltage. The extracted activation energy values for Ti/Au, Au, and Al/Au ZnO NW SB-FETs are of 0.29 eV (Ti), 0.28 eV (Au) and 0.23 eV (Al), respectively, as shown in Fig. 8. These values are close to the oxygen vacancy value reported and also have a good consistence with the extracted Schottky barrier height, suggesting that oxygen vacancies are the major defect levels in these ZnO NWs [19,21,22].

3.3.3. *ZnO NW surface states density extraction*

With the extracted activation energy (E_a) and trap temperature (T_t), the trap density *H* can be obtained by the following equation [26],

$$E_a = \frac{E_t}{k} \ln\left(\frac{qHL^2}{2\epsilon_{ZnO}\epsilon_0 V}\right) \quad (10)$$

where $E_t = kT_t$. The trap densities for Ti, Au, and Al contact devices are of $3.94 \times 10^{14}/cm^3$, $3.29 \times 10^{14}/cm^3$ and $3.42 \times 10^{14}/cm^3$, respectively. These trap densities, though very low, are high enough to influence metal contacts to ZnO NW. Theoretical investigations by the first principle calculations using density function theory predicted that the most location of oxygen vacancies in ZnO NWs is on the NW surface. The energy of oxygen vacancies on the NW surface is significantly lower than that in the NW center by as much as ~1 eV [29]. Therefore, in this study, the above trap densities are really the oxygen vacancy densities at the NW and metal contact interfaces. With a diameter of 100 nm, the interface trap densities for Ti, Au, and Al contact devices are $1.24 \times 10^{10}/cm^2$, $1.04 \times 10^{10}/cm^2$ and $1.07 \times 10^{10}/cm^2$, respectively. It is noted that the trap density values are at the same order and weakly dependent on the metal contacts, suggesting that the presence of oxygen

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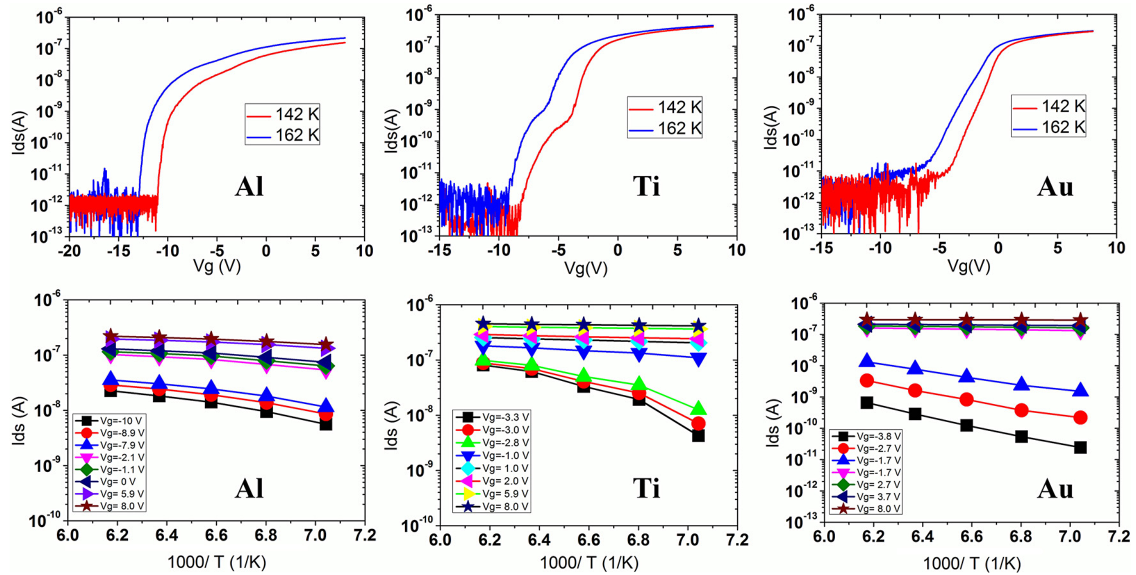

Fig. 7. Temperature dependent I_{ds}–V_g transfer characteristics for (a) Al/Au, (b) Ti/Au, and (c) Au contacted ZnO NW FETs from 142 K to 162 K at V_{ds} = 0.3 V. Drain current in log scale is approximately linear versus 1000/T in the gate bias range picked for activation energy extraction for (d) Al/Au, (e) Ti/Au, and (f) Au contacted ZnO NW FETs.

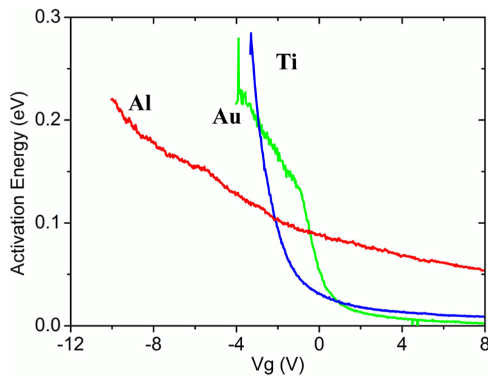

Fig. 8. Activation energy extracted from slope of Arrhenius plot versus gate voltage at V_{ds} = 0.3 V. The activation energy of Ti/Au, Au and Al/Au contacts are 0.29 eV (Ti at V_{gs} = −3.3 V), 0.28 eV (Au at V_{gs} = −3.7 V) and 0.23 eV (Al at V_{gs} = −9.99 V), respectively.

vacancies likely results in metal–Zn dangling bonds at the metal NW interface.

As shown above, a quantitative analysis of ZnO NW surface states can be accomplished by cryogenic I–V characterization of ZnO NW SB-FETs. The extracted activation energy provides a picture of the NW surface states distribution in energy domain. These are the surface states that affect electron transport in ZnO NWs the most. Combining the Schottky barrier heights extracted from room temperature I–V characterization, we have established a self-consistent method to investigate NW surface states here. The density of ZnO NW surface states can also be quantitatively extracted by space-charge-limited modeling.

4. Conclusions

In conclusion, we have shown that ZnO NW surface analysis from I–V characterization of ZnO NW SB-FETs. Both the energy level and density of NW surface states can be extracted from the method we present here without going through complex device fabrication and measurement process. Our results show that the Fermi level is pinned by ZnO NW surface states leading to an SBH of 0.34–0.37 eV. The trap temperature is around 150 K, below which the electron transport is space charge limited. The method developed in this work gives an effective way to characterize some intrinsic properties of semiconductor NWs.

Acknowledgements

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