Electric Stress-Induced Threshold Voltage Instability of Multilayer MoS_2 Field Effect Transistors

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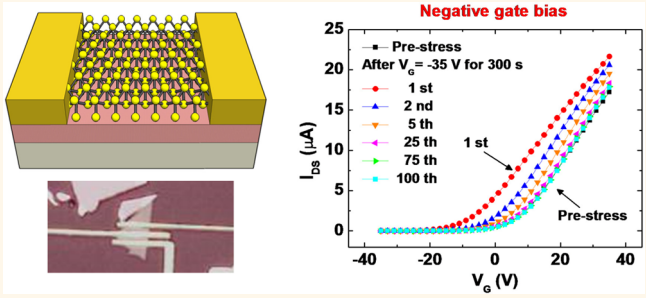
ABSTRACT We investigated the gate bias stress effects of multilayered MoS_2 field effect transistors (FETs) with a back-gated configuration. The electrical stability of the MoS_2 FETs can be significantly influenced by the electrical stress type, relative sweep rate, and stress time in an ambient environment. Specifically, when a positive gate bias stress was applied to the MoS_2 FET, the current of the device decreased and its threshold shifted in the positive gate bias direction. In contrast, with a negative gate bias stress, the current of the device increased and the threshold shifted in the negative gate bias direction. The gate bias stress effects were enhanced when a gate bias was applied for a longer time or when a slower sweep rate was used. These phenomena can be explained by the charge trapping due to the adsorption or desorption of oxygen and/or water on the MoS_2 surface with a positive or negative gate bias, respectively, under an ambient environment. This study will be helpful in understanding the electrical-stress-induced instability of the MoS_2-based electronic devices and will also give insight into the design of desirable devices for electronics applications.



KEYWORDS: molybdenum disulfide · field effect transistor · electronic transport · gate bias stress

Two-dimensional (2D) nanomaterials with layered structures, such as graphene, are of considerable interest as promising materials for next-generation nanoelectronic device applications because of their unique properties and the ability to easily fabricate complex structures.[1,2] Among the layered materials, molybdenum disulfide (MoS_2) has recently attracted a lot of attention due to its intriguing electrical and optical properties compared to the substantial limitations of graphene in electronic transistors.[3,4]

Unlike graphene, which does not have a band gap, bulk MoS_2 is a semiconductor with an indirect band gap of 1.2 eV, and single-layer MoS_2 is a semiconductor with a direct band gap of 1.8 eV.[5,6] Furthermore, MoS_2 has other excellent characteristics such as optical sensitivity and mechanical flexibility.[7−10] Accordingly, there have been considerable efforts into fabrication and characterization of MoS_2-based field effect transistors (FETs), sensing devices, memory devices, and logic circuits for future electronics and optoelectronics.[4,11−18] For example, single-layer MoS_2 transistors with a high on/off ratio of 10^8 have recently been demonstrated using HfO_2 as the top gate dielectric.[4] Additionally, multilayer MoS_2 transistors exhibiting high mobility (>100 $cm^2/(V\ s)$), near-ideal subthreshold swing (~70 mV/decade), and robust current saturation over a large voltage window have also been demonstrated.[18]

Despite these merits, large variations in the transport properties of MoS_2 FET devices due to extrinsic effects, such as absorption of oxygen and/or water from the environment, can result in limitations for exploring their intrinsic properties and overall stability.[19−22] Very recently, Late *et al.* showed that the hysteresis effects of MoS_2 FET devices measured under an ambient environment were presumably due to extrinsic/environmental effects, especially absorption of moisture on the surface.[21] Qiu *et al.* showed that because the MoS_2

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FET devices were sensitive to oxygen in the ambient environment, exposure to ambient conditions dramatically reduced the on-state current due to the additional scattering centers at the defect sites of MoS_2 caused by chemisorption.[22] They also demonstrated that vacuum annealing could effectively remove the adsorbates and reversibly recover the FET device performance.[22] Although there have been a number of reports on MoS_2 FET devices, the FET device stability under electrical stress has not yet been fully investigated. Understanding the electrical-stress-induced stability is very important in MoS_2-based FETs for developing appropriate device operation schemes for use in practical electronic devices.

Here, we investigated the electrical-stress-induced instability of multilayered MoS_2 FETs with a back-gated configuration under ambient conditions. For example, we studied the device's characteristics in response to a positive or negative gate bias stress (±35 V). The current of the device decreased (increased) and its threshold shifted in the positive (negative) gate bias direction with positive (negative) gate bias stress. We also studied the device's characteristics with different gate bias stress times, different gate bias sweep rates, and different gate sweep ranges. We compared the gate bias stress effects of the device in the ambient environment and in a vacuum.

RESULTS AND DISCUSSION

The MoS_2 flakes used in this study were prepared by the micromechanical exfoliation of a bulk MoS_2 crystal (purchased from SPI Supplies, USA). The exfoliated MoS_2 flakes were transferred to a 100-nm-thick SiO_2 layer on a highly doped p++ Si substrate that can be used as a back gate. After the MoS_2 flakes were transferred to the substrate, we located a suitable MoS_2 nanosheet that was a few layers thick using an optical microscope (see the atomic force microscope (AFM) image and cross-sectional profile in the Supporting Information, Figure S2). Then, to fabricate a MoS_2 FET device, the MoS_2 nanosheet was patterned using electron beam lithography. After patterning, Au (100-nm-thick)/Ti (10-nm-thick) was deposited as the source and drain electrodes using an electron beam evaporator. Using these methods, we made three MoS_2 FET devices. However, for the systematic study and comparison, all the data presented in this study were from one device. Detailed information of the device fabrication is explained in the Methods and Supporting Information (Figure S1).

Figure 1(a) shows a schematic of a MoS_2 FET with an optical image of the real device used in this study. Figure 1(b) displays the representative transfer characteristics (source−drain current *versus* gate voltage, $I_{DS}-V_G$) measured at a fixed source−drain voltage (V_{DS} = 0.1 V). The inset of Figure 1(b) shows the output characteristics (source−drain current *versus* source−drain

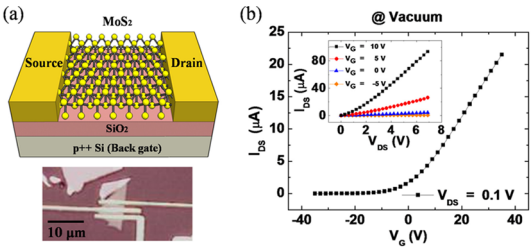

Figure 1. (a) Schematic of the MoS_2 FET. An optical image of a real device is also shown. (b) $I_{DS}-V_G$ curve measured at a fixed V_{DS} = 0.1 V in a vacuum. The inset shows $I_{DS}-V_{DS}$ for different V_G.

voltage, $I_{DS}-V_{DS}$) measured at different gate voltages (V_G = 10, 5, 0, and −5 V). These data were measured in a vacuum (~5.6 × 10^{-5} Torr). The device exhibited n-channel FET behavior because positive gate voltages increased the current. From the transfer characteristics (Figure 1(b)), we estimated a field effect mobility (μ) of ~25.7 $cm^2/(V\ s)$ using the following formula, $\mu = [dI_{DS}/dV_G] \times [L/(WC_iV_{DS})]$,[23] where $W = 6.3\ \mu m$ is the channel width, $L = 0.9\ \mu m$ is the channel length, and $C_i = \varepsilon_o\varepsilon_r/d \approx 3.5 \times 10^{-4}\ F/m^2$ is the capacitance between the active layer and the back gate per unit area. Here, ε_r is the dielectric constant of SiO_2 (~3.9), ε_o is the vacuum permittivity, and d is the SiO_2 thickness (100 nm). Previous studies have reported that the mobility of single-layer MoS_2 FETs is in the range from 0.1 to ~200 $cm^2/(V\ s)$.[4,18,19,24,25]

We investigated the threshold voltage instability for the MoS_2 FET device under various gate bias stresses. To investigate the effect of the gate bias stress on the electronic properties of the device, we first applied a constant gate bias for 300 s, and then we measured 100 transfer characteristic curves consecutively. Figure 2(a,b) display these repeated measurement results. First, the data were obtained (black curve, denoted as "pre-stress"), then a constant +35 V (Figure 2(a)) or −35 V (Figure 2(b)) gate bias stress was applied for 300 s, and finally, 100 consecutive data points were measured. After the positive gate bias stress, the source−drain current decreased significantly and the threshold voltage of the device shifted in the positive gate bias direction (see the data labeled "1st" in Figure 2(a)). Then, the current gradually increased and the threshold voltage shifted in the negative gate bias direction, and eventually, the curve approached the original state (pre-stress curve). In contrast, for the negative gate bias stress, the current increased and the threshold voltage shifted in the negative gate bias direction (see the data labeled "1st" in Figure 2(b)). Then, the current gradually decreased and the threshold voltage shifted in the positive gate bias direction, and similar to the positive gate bias stress, the curve returned to the original state (pre-stress curve). Figure 2(c) shows the shift in the threshold voltage at each measurement with respect to the value for the pre-stress curve. Here, the threshold voltage is the value

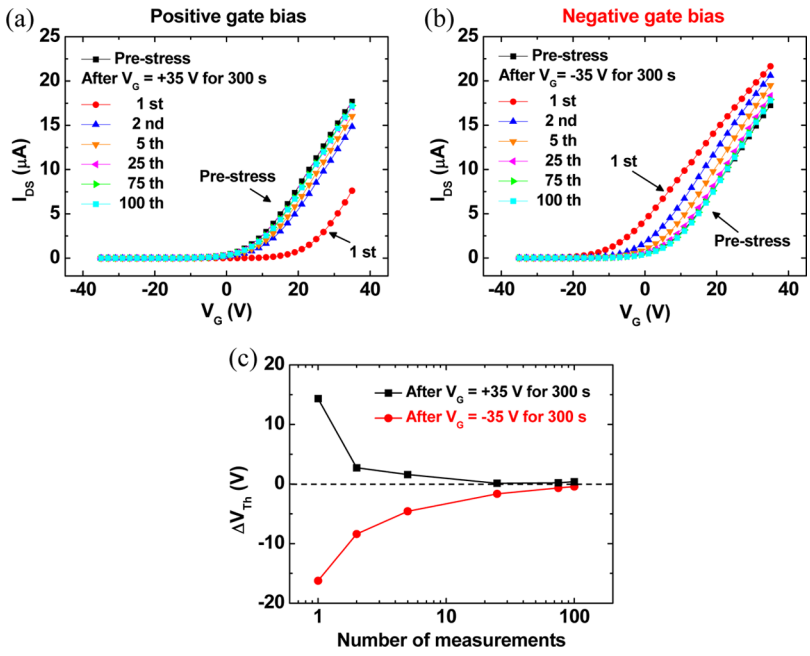

Figure 2. (a, b) $I_{DS}-V_G$ curves ("pre-stress") measured before the gate bias stress and 100 consecutive $I_{DS}-V_G$ curves right after (a) +35 V gate bias stress and (b) −35 V gate bias stress was applied for 300 s. Data were measured in ambient conditions. (c) Shift of the threshold voltage (ΔV_{Th}) for each measurement with respect to the value of the pre-stress curve.

of the gate bias when the channel just begins to allow significant current to flow; we determined the threshold voltage from the *x* (gate voltage)-axis intercept obtained from the linear fitting of the linear parts of the characteristic transfer curves.[23,26] With V_{Th} determined, we also estimated the carrier density of the device (see details in Figure S5 in the Supporting Information).

These phenomena (Figure 2) can be attributed to charge trapping due to the adsorption of oxygen and/or water in an ambient environment at defect sites on the MoS_2 surface.[19,20,22] Charge trapping under a positive gate bias stress can be enhanced by an increase in the adsorption of oxygen and/or water at the MoS_2 channel surface due to the increase in electrons caused by the positive gate bias. The charge trapping results in a decrease in the electrical conductance and causes the threshold voltage shifts in the positive gate bias direction. The electrons trapped on the MoS_2 surface can be released by applying a negative gate bias, which results in an increase in the conductance, and the threshold voltage shifts toward the negative gate bias direction. Similar behaviors have been observed in other types of nanoelectronic devices made with ZnO nanowires, InGaZnO(IGZO) films, and graphene.[27−33] Unlike such materials-based FETs, the threshold voltage instability in Si-based FETs can be explained mainly in terms of defect state creation and charge trapping effect at the interface between channel layer and dielectric layer under electrical stresses.[34−36] In our experiments, the adsorption/desorption of oxygen and water molecules on the MoS_2 surface under ambient environment starts to play dominant roles in the electrical transport properties of MoS_2 FETs.

We also investigated the effect of the gate bias stress time on the same device in ambient conditions. Figure 3(a) presents the transfer characteristic data (at V_{DS} = 0.1 V) of the device obtained right after we applied a constant +35 V gate bias for different gate bias stress times that varied from 0 to 500 s with a fixed gate bias sweep rate of 8 V/s. The inset of Figure 3(a) shows the logarithmic plot. For example, the data labeled "10 s" were obtained after we applied a +35 V gate bias for 10 s. We waited about an hour before each measurement to ensure that the device fully recovered from the previous gate bias stress. We confirmed that the data were fully recovered; in other words, the measured data were almost the same after waiting an hour for all gate bias stresses. Please see the two "0 s" curves in Figure 3(a,b), which are very similar because the waiting time was sufficient for the device to fully recover. From Figure 3(a), one can see that under a positive gate bias stress the current decreased and the threshold voltage shifted in the positive gate bias direction.

We repeated the gate bias stress measurements with a negative gate bias. Figure 3(b) displays the transfer characteristics data obtained after we applied a constant −35 V gate bias for different times while all the other conditions were the same as in Figure 3(a). For the negative gate bias stress (Figure 3(b)), the current increased and the threshold voltage shifted in the negative gate bias direction. The results in Figure 3 are consistent with the observed results in Figure 2: a positive (negative) gate bias stress decreased (increased) the current and the threshold voltage shifted in the positive (negative) gate bias direction. These observations are

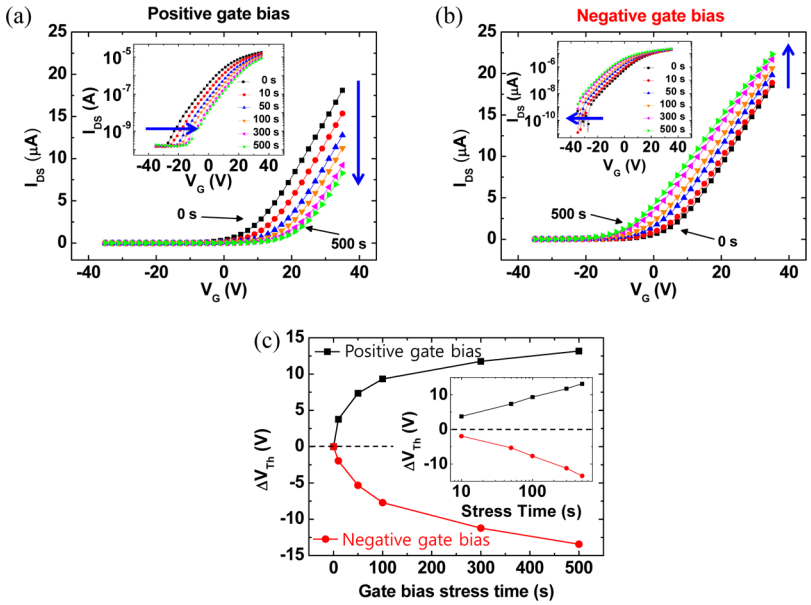

Figure 3. (a, b) $I_{DS}-V_G$ curves measured in ambient conditions after (a) +35 V and (b) −35 V gate bias stress was applied for different stress duration times. (c) Shift in the threshold voltage (ΔV_{Th}) for each measurement with respect to the value for the initial curve ("0 s" curve). The inset is the plot made on the logarithmic scale of stress time.

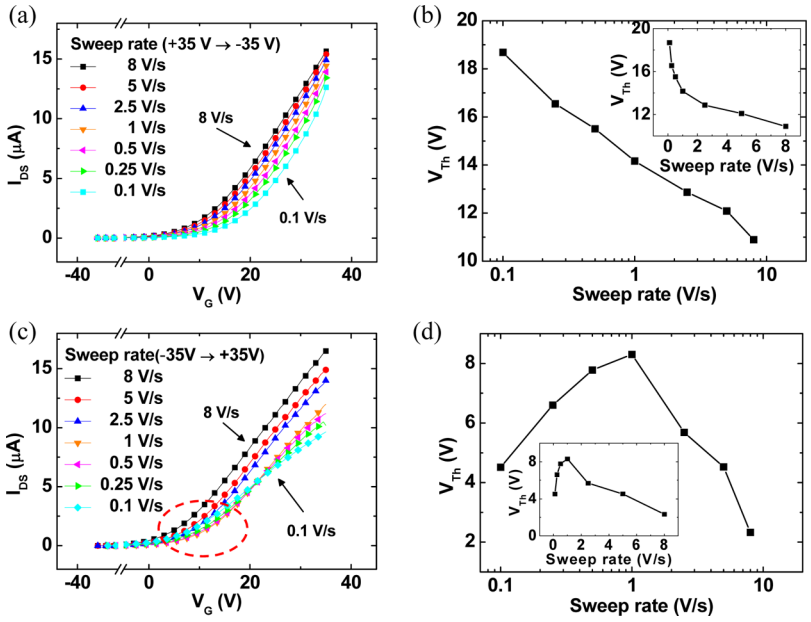

Figure 4. (a, c) $I_{DS}-V_G$ curves measured in ambient conditions with different gate bias sweep rates ranging from 8 to 0.1 V/s. The gate bias was swept (a) from +35 to −35 V and (c) from −35 to +35 V. (b, d) Threshold voltage (V_{Th}) at each measurement for different sweep rates for gate bias swept (b) from +35 to −35 V and (d) from −35 to +35 V. Insets in (b) and (d) are plots made as the linear scale of sweep rate.

due to the charge trapping associated with the ambient effect. The shift in the threshold voltages at each measurement as a function of the gate bias stress time for both the positive and negative gate biases was plotted in Figure 3(c). The inset in Figure 3(c) is the logarithm time scale. One can see that the shift in the threshold voltage increased with respect to the value for initial curve (0 s) as the gate bias stress time increased for both gate bias polarities. When the gate bias is applied for a long enough duration, the absorbed oxygen and/or water will be saturated and the shift in the threshold voltage will also be saturated.

We also examined the effect of the gate bias sweep rate on the device's characteristics. Figure 4(a) shows the transfer characteristics measured at ambient conditions with a gate bias sweep from +35 V to −35 V at different sweep rates (from a fast rate of 8 V/s to a slow rate of 0.1 V/s). As shown in Figure 4(a), as the sweep rate decreased, the current decreased, and the threshold voltage shifted in the positive gate bias direction.

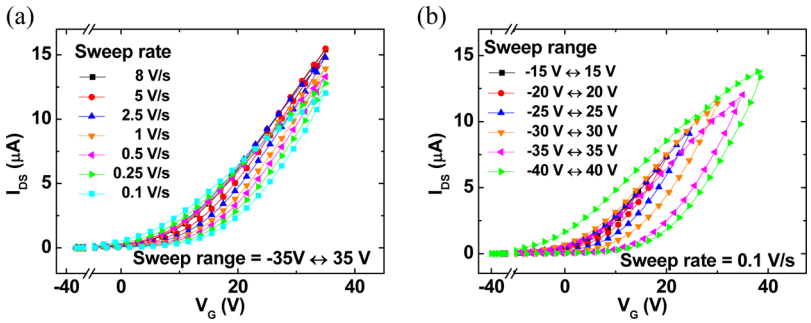

Figure 5. (a) Hysteresis $I_{DS}-V_G$ curves of double sweep (from −35 to +35 V and then back to −35 V) at different gate bias sweep rates measured in the ambient environment. (b) Hysteresis $I_{DS}-V_G$ curves with different gate bias sweep range at a fixed gate bias sweep rate of 0.1 V/s in ambient.

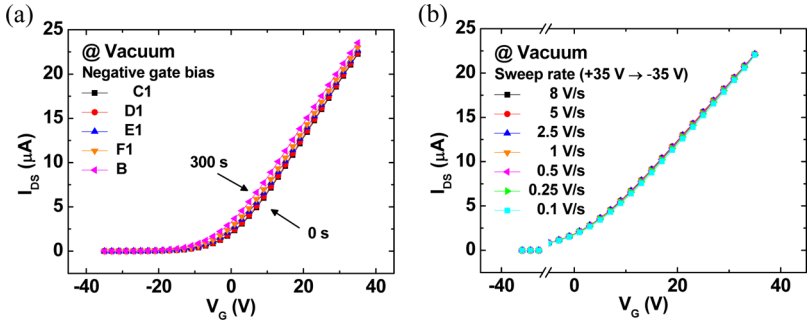

Figure 6. (a) $I_{DS}-V_G$ curves measured in a vacuum after −35 V gate bias stress was applied for different stress duration times. (b) $I_{DS}-V_G$ curves measured in a vacuum during the gate bias sweep from +35 to −35 V with different gate bias sweep rates.

The positive shift of the threshold voltage as the sweep rate decreased can be observed in the logarithmic scale (Figure 4(b)) and linear-scale plot (Figure 4(b) inset). This behavior is consistent with the data in Figures 2(a) and 3(a) because a slow sweep rate means a longer gate bias stress time. Similar behavior was observed in the case of the opposite gate bias sweep direction (*i.e.*, the sweep from −35 V to +35 V with the same sweep rate conditions), as shown in Figure 4(c,d). As the sweep rate decreased, the current also decreased, and the threshold voltage shifted in the positive gate bias direction as a result of the longer stress time of the positive gate bias at the slower sweep rates. However, at the slower sweep rates of 0.5, 0.25, and 0.1 V/s, the current first increased around a low gate bias (circled in Figure 4(c)), then it decreased at larger positive gate bias. This can be explained by considering the positive and negative gate bias sweep ranges separately; at slower rates, when the gate bias was swept from −35 to 0 V, the current tended to increase first (consistent with the case of Figures 2(b) and 3(b)), and then when the gate bias was continuously swept from 0 V to +35 V, the current decreased (consistent with the case of Figures 2(a) and 3(a)). This phenomenon resulted in an increase and then decrease in the threshold voltage as the sweep rate slowed (from 8 V/s to 0.1 V/s), as shown in Figure 4(d).

Figure 5 displays the effect of gate bias double sweeps, *i.e.*, −35 to +35 V and then back to −35 V, at the same sweep rates. The results are shown in Figure 5(a). As the sweep rate decreased, the current tended to increase in the negative gate bias range (−35 to 0 V) and to decrease during the positive gate bias range (0 to +35 V); thus, there is a hysteresis in the double sweep loop. This hysteresis effect became more obvious at the slower sweep rates because the slower sweep rates (*i.e.*, longer gate bias time) enhanced the gate bias stress effects. Similarly, this hysteresis effect became more significant as the gate bias sweep range increased (Figure 4(b)).

To investigate the ambient effect, we repeated the gate bias stress measurements in a vacuum (5.6×10^{-5} Torr). Figure 6(a) shows the transfer characteristic curves that were measured in a vacuum with the same measurement conditions as the data in Figure 3(b). Figure 6(b) shows the data measured in a vacuum at the same conditions as the data in Figure 4(a). No significant gate bias stress effects were observed in the vacuum environment. There were small shifts observed in the data, especially in Figure 6(a). These shifts are due to the interfacial traps at the interface between the MoS_2 and SiO_2 dielectric layer in response to the gate bias stress.

Next, we discuss the gate bias stress effect on the MoS_2 FET using energy band diagram schematics. Figure 7 shows the energy band diagram for V_{SD} = 0 V and V_G = 0 V at ambient conditions for three cases: no gate bias stress, positive gate bias stress, and negative gate bias stress. To understand the charge transport, we need to consider the metal/MoS_2 contact interfaces at the source and drain electrodes because metal contacts to semiconducting MoS_2 can create

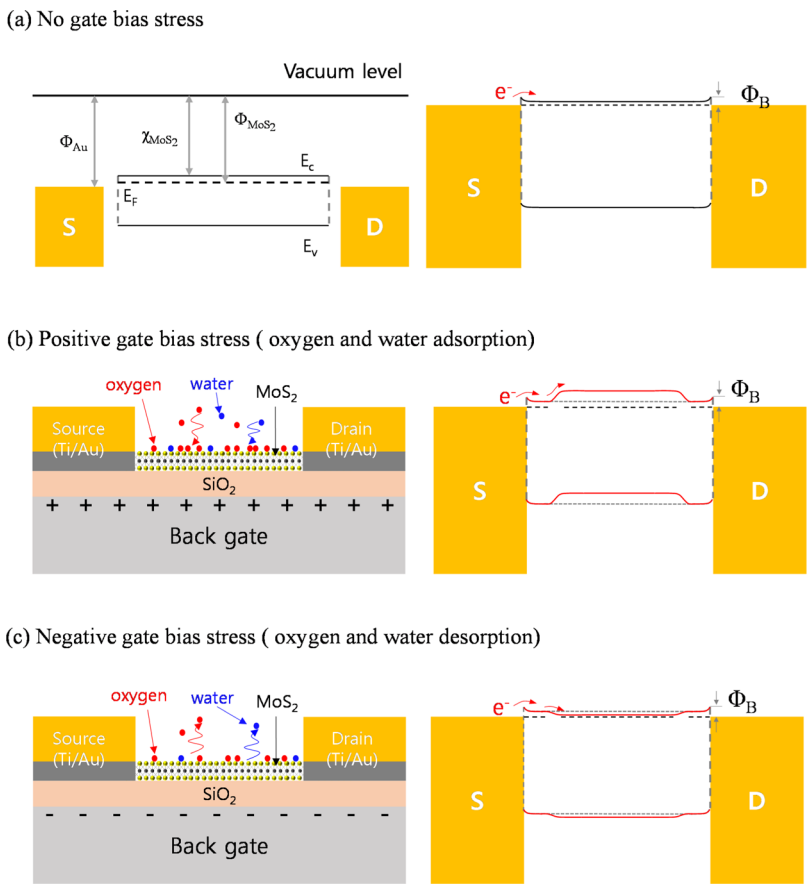

Figure 7. Schematics of the energy band diagram at V_G = 0 V in the ambient environment when (a) no gate bias stress, (b) positive gate bias stress, and (c) negative gate bias stress is applied.

Schottky barriers, which can dominate the electronic properties of MoS_2-based devices. We first assume that although a band gap of MoS_2 is dependent on their thickness, our MoS_2 nanoflakes have a band gap of about 1.2 eV, similar to that of the bulk. In addition, MoS_2 has an electron affinity of 4.0 eV,[37,38] a work function of 4.6−4.9 eV.[39,40] Contact metals used as source and drain electrodes in our study are Ti and Au, with work functions of 3.9−4.3 and 5.1−5.4 eV, respectively. Because the Ti layer is an adhesion layer for Au contact to a MoS_2 nanoflake, we considered the band alignment of Au-MoS_2 interfaces at the source and drain. According to Popov *et al.*,[41] the Ti can play a role in modifying the interface properties due to an increase in the density of state at the Fermi level (E_F), resulting in a low-resistance ohmic contact. Our results clearly indicate that the MoS_2 FET device exhibits the typical n-type semiconducting behavior with low-resistance ohmic contact at low voltages in the output curves (see $I_{DS}-V_{DS}$, the inset of Figure 1(b)), which is consistent with previous results.[38,39,42] Accordingly, we can consider the band alignment for the Au/MoS_2 contacts at the source and drain with a very small Schottky barrier (Φ_B), as shown in Figure 7(a). Here, we assume that the gate bias stress effects can be due to the adsorption/desorption of oxygen and water on the MoS_2 surface, and the MoS_2 region underneath the metal contact is not affected by such adsorption/desorption. In the case of the application of identical positive gate bias stress, the accumulated electron density in the channel region increases by positive electric field and the resulting adsorbed oxygen and water concentration on the MoS_2 channel surface is also increased, in which the adsorbed oxygen and water can capture charge carriers from the conduction band in the MoS_2 channel. This causes channel depletion and the observed positive V_{Th} shift (Figures 2(a) and 3(a)). As shown in Figure 7(b), carriers first travel through the interface region between the MoS_2 and metal contact and then traverse the channel depletion-induced conduction barrier before entering into the MoS_2 channel. In contrast, when a negative gate bias stress is applied, oxygen and water desorb in response to the identical negative gate electric field. The electrons that are trapped by the adsorbed oxygen and water at the MoS_2 channel region are released and transferred to the MoS_2 channel by the application of negative gate bias stress, which results in a reduction of the carrier depletion of the MoS_2 FET. As shown in Figure 7(c), the desorption of oxygen and water causes the accumulation of charge carriers from the conduction band in the MoS_2 channel, leading to the observed

negative V_{Th} shift (Figures 2(b) and 3(b)). These results suggest that the passivation of the MoS_2 surface will be important to obtain reproducible results and to minimize the ambient effect.

CONCLUSION

We investigated the electrical-stress-induced threshold voltage instability of multilayered MoS_2 FET devices with a back-gated configuration under an ambient environment. When a positive (negative) gate bias stress was applied to the device, the current decreased (increased) and the threshold shifted in the positive (negative) gate bias direction. This effect was enhanced when a longer gate bias time or a slower sweep rate of the gate bias was applied. These gate bias stress effects can be explained by the charge trapping mainly due to the adsorption (desorption) of oxygen and/or water on the MoS_2 surface with a positive (negative) gate bias under ambient conditions. Our study has important implications for a better design of functional nanodevices based on two-dimensional layered calcogenides for wide nanoelectronic device applications.

METHODS

The multilayer MoS_2 active layer used in this study was exfoliated using the micromechanical exfoliation method from a bulk MoS_2 crystal purchased from SPI Supplies. Then, the multilayer MoS_2 flakes were transferred from 3M Scotch tape to SiO_2 on a heavily doped p++ Si wafer (resistivity $\sim 5 \times 10^{-3}$ Ω cm) that can be used as a back gate. After finding the location of a multilayer MoS_2 flake using an optical microscope, the MoS_2 nanosheet's height was measured with a NX 10 AFM system (Park Systems). To make patterns of electrodes, we spin-coated methyl methacrylate (9% concentration in ethyl lactate) and poly(methyl methacrylate) 950K (5% concentration in anisole) at 4000 rpm. After the spin-coating of each layer, the sample was baked at 180 °C for 90 s. The electrodes were patterned using an electron beam lithography system (JSM-6510, JEOL) with a 30 kV exposure. The pattern development was performed with an methyl isobutyl ketone/isopropyl alcohol (1:3) solution with a development time of 50 s. The electrical characteristics of the device were measured using a semiconductor parameter analyzer (HP 4145B) in a probe station (JANIS model ST-500).

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Additional information including device fabrication details, AFM and optical images, effect of gate bias stress on the device under vacuum, and estimation of the carrier concentration. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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Figure 6(a) correction