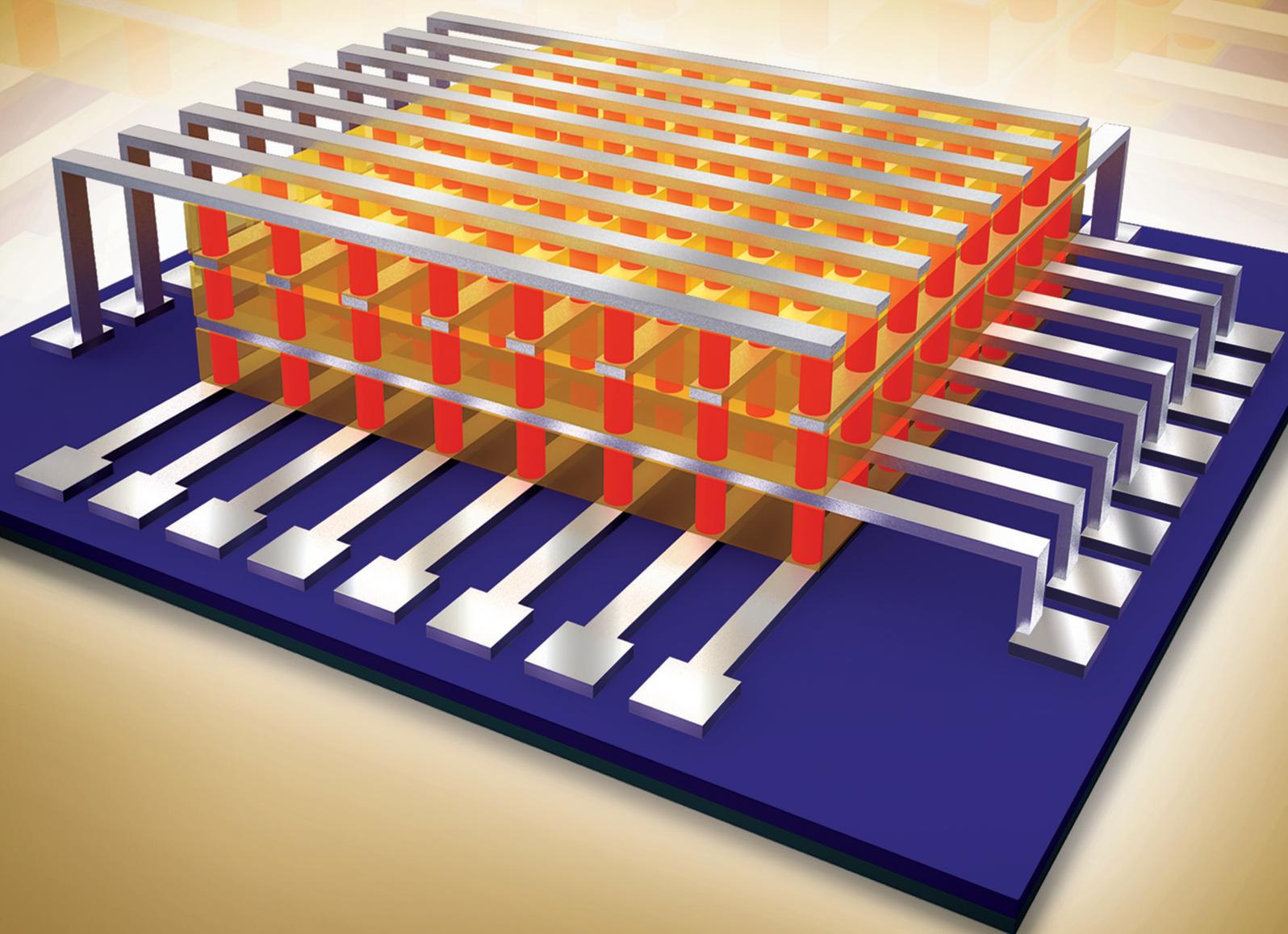


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ADVANCED MATERIALS



Three-Dimensional Integration of Organic Resistive Memory Devices

By Sunghoon Song, Byungjin Cho, Tae-Wook Kim, Yongsung Ji, Minseok Jo, Gunuk Wang, Minhyeok Choe, Yung Ho Kahng, Hyunsang Hwang, and Takhee Lee*

Since the discovery of conducting polymers^[1], organic-based electronics such as organic light-emitting diodes, transistors, photovoltaics, and memory devices have been spotlighted as potentially innovative devices given their easy and low-cost fabrication by spin-coating or ink-jet printing, and their flexibility.^[2–15] Among these, organic memories have been extensively investigated for data-storage application.^[11,14,16–21] However, organic memories so far have been fabricated in single cells or in arrayed cells with low memory cell density^[22–29], which constitutes an obstacle to their more practical application. In this regard, the three-dimensional (3D) stacking of memory devices provides a way to achieve a great increase in memory cell density. Unlike silicon or inorganic-based memory devices, which can be fabricated in complicated vertically stacked multi-layers, organic devices are built from organically active—and thus chemically unstable in multi-layer stacking—materials that are not trivial to stack. The success of multi-layer stacked device fabrication by the spin-coating process depends to a great extent on the chemical and thermal robustness of the organic material^[30] because the stacked over-layer may dissolve the below-layer with excess solvent during the spin-coating.

Here we demonstrate the fabrication of 3D-stacked 8×8 cross-bar array polymer resistive memory devices with a composite of polyimide (PI) and 6-phenyl-C61 butyric acid methyl ester (PCBM) as the memory element by using simple spin-coating processes to deposit the active layers. Individual memory cells in the different layers can be independently controlled and monitored and they exhibited excellent memory performance in terms of ON/OFF ratio, cycling, and retention time. Our demonstration of 3D stackable organic memory devices will bring closer the prospect of achieving highly integrable organic memory devices and other organic-based electronics.

A conceptual schematic of the 3D-stacked 8×8 crossbar multi-layer organic memory devices is illustrated in **Figure 1a**.

In the crossbar structure, which is an effective architecture for multi-layer stacking, bit-lines and word-lines cross each other perpendicularly and the active (PI:PCBM) memory elements are placed between them. In 3D-stacked cross-bar architecture, the bit- and word-lines are designed to function as both the top electrodes of the memory cells beneath them and the bottom electrodes of the cells above them.^[31,32] Each organic active layer (yellow layers in Figure 1a) is spin-coated between two Al electrode layers. The devices in our study have three active organic memory layers and a total of $64 \times 3 = 192$ produced memory cells; these are depicted as orange pillars in Figure 1a. Figure 1b shows a cross-sectional transmission electron microscopy (TEM) image of a three-layer stacked memory devices assembly fabricated as part of this study. The image shows well-separated PI:PCBM active layers stacked between the bit- and word-line Al electrodes (see Figure S3–S5 in the Supporting Information). The devices were subjected to a repetitive curing process carried out at over 300 °C to harden the organic layers and prevent their intermixing during the fabrication (see Experimental, Figure S1 and S2, Supporting Information for more details of the fabrication process). Figure 1c shows the chemical structures of the organic active materials (cured PI and PCBM) used in this study.

All the memory cells in the stacked assembly were electrically examined in order to analyse their memory characteristics. **Figure 2** shows representative semilogarithmic current-voltage (I – V) curves resulting from measurements on selected memory cells in the first (Figure 2a), second (Figure 2b), and third (Figure 2c) active layers of the 3D-stacked assembly. The actual locations of the memory cells appear as red marks in the insets. All three sets of cells clearly exhibit similar—and typical—unipolar-type memory switching characteristics, with the resistive switching occurring within the same bias polarity.^[28] To switch the device from the initial high-resistance state (HRS or OFF state) to the low-resistance state (LRS or ON state), the voltage was swept from 0 to 5 V and then from 5 to 0 V in sequence; this *set* process corresponds to the 1st curves in the Figure. When the applied voltage increased beyond the threshold voltage $V_{th} \sim 3.8$ V, the current level abruptly increased by more than three orders of magnitude. Once the device was turned on from the HRS to the LRS, the LRS was well maintained even after the applied voltage was removed, signalling non-volatile memory behavior. The device was switched from the LRS back to the HRS by sweeping the voltage singly from 0 to 10 V (the *reset* process, corresponding to the 2nd curves in the Figure). During the reset process, the current increased until it attained a maximum at $V_{max} \sim 3.1$ V in the LRS curve trace; subsequently a negative differential resistance (NDR) was observed in the range

[*] S. Song, B. Cho, Dr. T.-W. Kim,† Y. Ji, M. Jo, G. Wang, M. Choe, Dr. Y. H. Kahng, Prof. H. Hwang, Prof. T. Lee
Department of Materials Science and Engineering
Gwangju Institute of Science and Technology
Gwangju, 500–712 (Korea)
E-mail: tlee@gist.ac.kr

Prof. H. Hwang, Prof. T. Lee
Department of Nanobio Materials and Electronics
Gwangju Institute of Science and Technology
Gwangju, 500–712 (Korea)

[†] Present Address: Department of Materials Science and Engineering,
University of Washington, Seattle, Washington, 98195 (USA)

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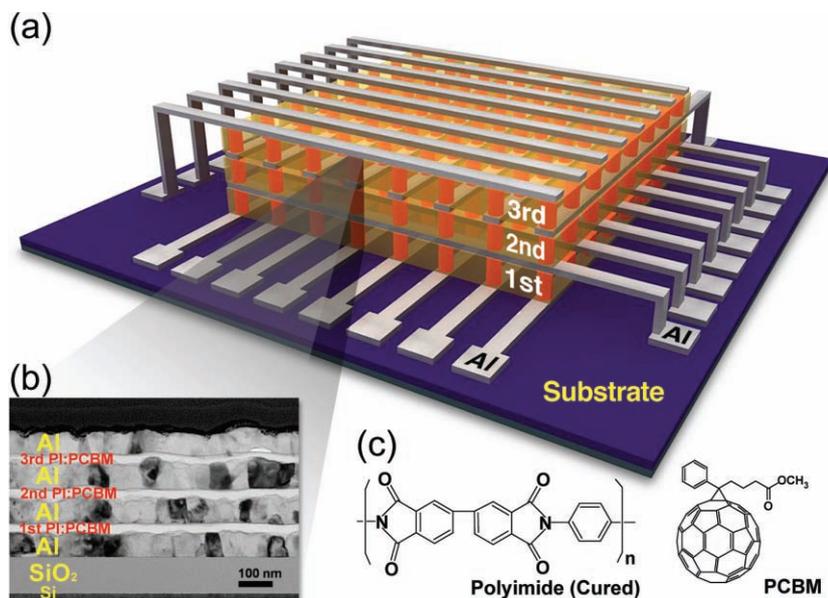


Figure 1. (a) Schematic illustration of a 3D-stacked organic resistive memory assembly featuring a 8×8 crossbar structure. A total of 192 cells (coloured orange) were produced in three active layers (coloured yellow) sandwiched between pairs of Al electrode layers. (b) Cross-sectional TEM image of the stacked device highlighting the three layers of organic memory cells. (c) The chemical structures of cured PI and PCBM used as the memory material.

from V_{\max} to V_{\min} . Such electrical resistive switching properties can be explained by the charge-trapping mechanisms reported by Simmons and Verderber^[33] and by Bozano et al.^[34,35] Symmetric electrical switching characteristics were also observed in the negative-voltage region with the same absolute-value voltage conditions.^[22] (The 3rd and 4th curves in the Figure respectively represent the *set* and *reset* processes for this region.)

Figure 3 shows statistical data of the switching characteristics of all the memory cells in the three active layers. The illustration on the left-hand side of Figure 3a shows the three (yellow) organic memory layers sandwiched between pairs of (gray) Al electrode layers; the images on the right-hand side show how the operative (red) memory cells and those rendered inoperative by electrical short (and shown in black) were distributed in each active layer. Despite the loss of some cells, the memory assembly exhibited a high device yield; specifically, 56 cells out of 64 (or 87.5%) were operative as memory in the first and second active layers and 48 cells (75%) were operative as memory in the third layer, for an overall yield of 160/192 or 83.3% (see Figure S7–S9

in the Supporting Information). This suggests that the fabrication of 3D-stacked multi-layer crossbar organic memory arrays is possible, enabling the high-density integration of organic memory devices by the straightforward addition of layers. Although three layers were demonstrated here, in principle further stacking would be possible, thus increasing the memory cell density indefinitely. Note that the inoperative memory cells were found to lie along a common electrode line; this implies that performing measurements on inoperative memory cells damages the other cells on the same line and, consequently, that more-careful measurements particularly in the forming process might have saved more memory cells and increased the device yield further.

Figure 3b shows the cumulative probability of the switching currents of all the operative memory cells in each layer. Here, the current values measured at a read voltage of 0.3 V are plotted as the ON and OFF currents (see also Figure 2). The distribution of the ON current values is seen to lie within about an order of magnitude, while the distribution of the OFF current values is broader. The important point, however, is that the ON and OFF

currents are separated by more than one order of magnitude. Figure 3c displays the statistical distributions of the threshold voltages (V_{th}) of the operative memory cells in each layer. The threshold voltage is that at which the memory cell switches on; as seen in Figure 2, the transition from the HRS to the LRS occurs at voltages between 2.8 and 4.4 V. The threshold-voltage distributions are found to be similar from layer to layer, indicating that all the individual memory cells can be switched ON by a uniform parameter.

To examine in detail the memory performance of the 3D-stacked organic memory devices we performed a series of characterizations such as the write-read-erase-read cycle test, the dc sweep endurance test, and the retention test. **Figure 4a** shows representative data from the repeating cycle test; this consists of write, read, erase, and read cycles for selected memory cells in each layer. The input voltages in the test, shown in the top plot, were 100 ms, 5 V pulse as the write, a 100 ms, 10 V pulse as the erase, and 1 V as the read signal. As the write, read, erase, and read input voltage pulses were applied in sequence,

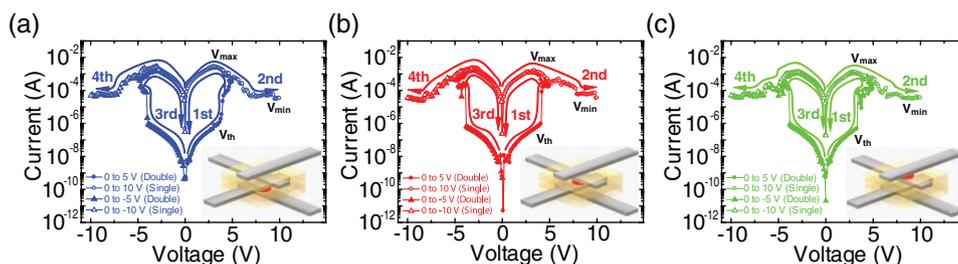


Figure 2. (a)–(c) I – V curves of selected memory cells from the first, second, and third active layers (shown from bottom to top). The red marks in the insets indicate the locations of the memory cells in the active layers. The I – V data displays unipolar-type switching behaviour.

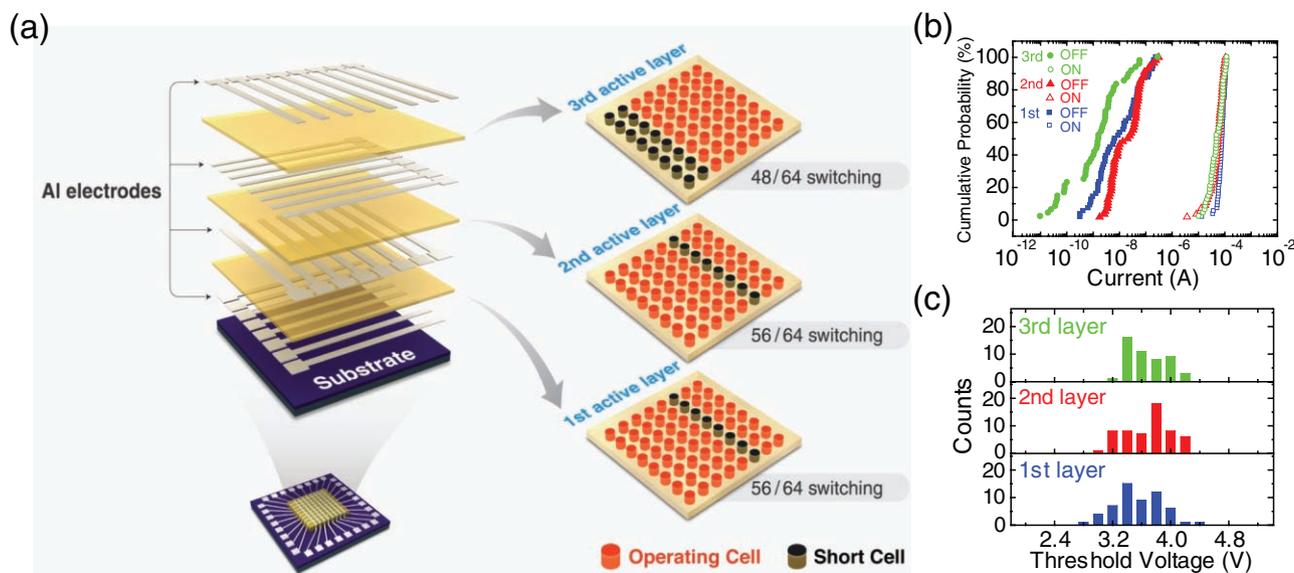


Figure 3. (a) Illustration of the 3D stacked memory assembly (left) and statistical distribution of the memory-operative cells (red) and the electrically shorted cells (black) in each active layer (right). (b) Cumulative probability data for all operative cells (160 operative cells out of 192 fabricated cells) (c) Statistical distribution of the threshold voltages of the operative cells in each active layer.

the memory cells in each layer responded with the ON and OFF output current values shown in the bottom three plots of Figure 4a. Figure 4b shows the results of the dc sweep endurance test. Dc voltage sweeps of about 60 times were performed under unchanging conditions to the memory cells in each layer. During the repetitive sweeps, our stacked memory devices maintained their ON/OFF ratios of over $\sim 10^3$ without showing

any significant electrical degradation. We also measured the retention times of the memory cells. The current values of the two states (ON and OFF) were measured at a read voltage of 0.3 V. As Figure 4c shows, the stacked memory devices had a good retention property over a 5×10^4 s test period and showed the extrapolated retention time over a year. In this retention test the ON/OFF current ratios were also maintained at over three orders of magnitude and did not exhibit any serious electrical

degradation. These excellent electrical performances suggest the basic potential, which is importantly related to possibility of 3D stacking application on the flexible substrates together with our previous study.^[36]

In summary, we have fabricated 3D-stacked 8×8 crossbar-structure organic resistive memory devices in which a composite of PI:PCBM was successfully employed as a thermally and chemically robust active organic material for stacked memory cells. The fabrication yields of the operating memory cells were more than 83% in the three-layer assembly reported here. The memory cells in each layer exhibited high performance with regard to non-volatile memory characteristics: they performed well under repetitive writing and erasing, had good switching endurance, and exhibited extrapolated memory retention times over a year with 10^3 ON/OFF current ratios. This study will enable highly integrated—and therefore more practical—organic memory devices and other organic-based electronic devices in the stackable 3D architecture with much increased cell density.

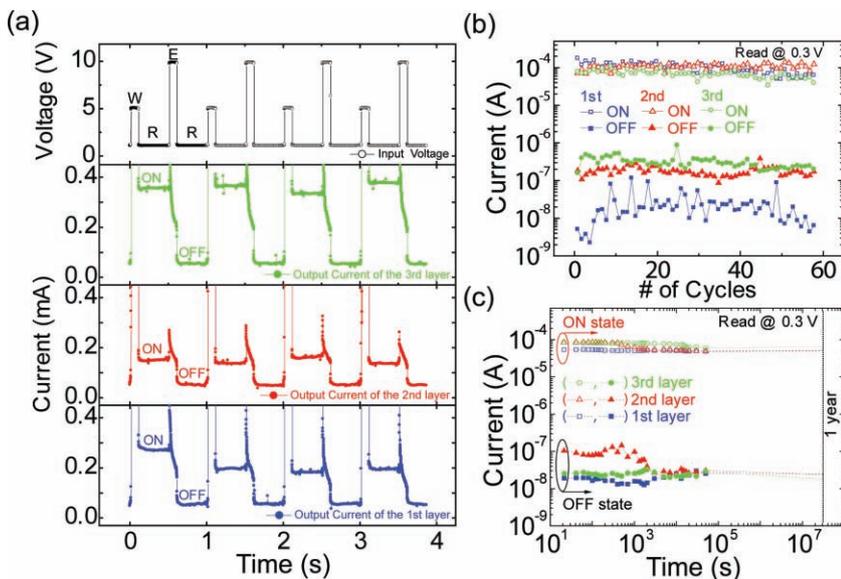


Figure 4. (a) Write-Read-Erase-Read cycle test data of the stacked organic memory assembly. The curve in the top panel indicates the input voltage pulses; the curves in the lower three panels depict the corresponding output current responses of selected memory cells in each layer. (b) The dc sweep endurance characteristics of the memory cells in each layer. (c) Retention-time test results of the ON and OFF states of the memory cells in each layer. The extrapolations of the data are also shown.

Experimental Section

For the spin-coating of the active layer of the organic resistive memory devices we used a composite solution consisting of polyimide (PI) and 6-phenyl-C61 butyric acid methyl ester (PCBM). The PI precursor, biphenyltetracarboxylic acid dianhydride p-phenylene diamine (BPDA-PPD), was dissolved in N-methyl-2-pyrrolidone (NMP) solvent with a BPDA-PPD:NMP-solvent weight ratio of 1:3. The PCBM was dissolved in the NMP solvent at a concentration of 0.5 wt%. Afterwards a composition solution of PI:PCBM was prepared using a 4:1 ratio of PI solution (2 ml) to PCBM solution (0.5 ml). Finally, the resulting mixed solution was filtered using polytetrafluoroethylene-membrane-based (PTFE) micro-filters with a pore size of 0.45 μm .

To fabricate the 3D-stacked crossbar-arranged 8×8 three-layer organic memory assembly we initially cleaned a Si/SiO₂ substrate in an ultrasonic bath using acetone, methanol, and de-ionized water in sequence for 10 minutes. To produce the bottom electrodes (BEs) we deposited Al using a shadow mask in an electron-beam evaporator and formed eight lines, each of width 200 μm and thickness 50 nm. The deposited BEs were then exposed to a UV-ozone treatment for 10 min in order to improve the reliable property of the organic resistive memory^[27] and adhesion between the metal and the organic active layers. At this point the PI:PCBM composite solution was spin-coated onto the Si/SiO₂/Al substrate at 500 rpm for 5 seconds and subsequently at 2000 rpm for 35 seconds. The coated organic film was soft-baked on a hot plate at 120 °C for 10 min so as to dry the solvent from the organic active layer. After the soft-baking, the contact pads of the BEs were exposed for the electrical measurements by swabbing with a cotton Q-tip soaked in methanol, and after that the organic active layer was hard-baked on a hot plate at 300 °C for 30 min to evaporate the residual solvent and to thermally cure the polymer composite. The whole process was carried out in a glove-box system filled with N₂. Cross-sectional TEM measurements yielded a ~25-nm thickness for the PI:PCBM active layer. The formation of the first active layer was followed by the deposition of the first intermediate Al electrodes; to realize our crosswise perpendicular design we rotated the initial shadow mask by 90°. The first set of intermediate Al electrodes are simultaneously the BEs of the second polymer active layer and the top electrodes (TEs) of the first polymer active layer. To form the second and third organic active layers we repeated the processes described above. The finished 3D stacked memory assembly consists of three layers of organic resistive memory cells, each containing 8×8 crossbar-type array of cells, for a total of 192 memory cells. (See Figure S1 and S2 for more details in the Supporting Information.) The current-voltage measurements were performed with using a semiconductor analyzer system (Model 4200-SCS, Keithley, Inc.) in a N₂-filled glove box system at room temperature. The write-read-erase-read cycles tests were measured using a two-channel pulse generator (Agilent Technology 81104A) and a two-channel oscilloscope (Tektronix TDS 3054B).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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