Tuning of the electronic characteristics of ZnO nanowire transistors and their logic device application

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ABSTRACT

We present the tuning of electrical characteristics of ZnO nanowire field effect transistors (FETs) by controlling surface morphology and size of nanowires and by introducing proton-irradiation-assisted manipulation and further demonstrate their logic inverter circuit. The FETs made from surface-architecture-controlled ZnO nanowires exhibit two different types of operation modes, which are distinguished as depletion and enhancement modes in terms of the polarity of the threshold voltage. We also explain that the electrical transport behaviors are associated with the influence of surface states. In addition, we demonstrate the proton irradiation effects on the electrical characteristics of two different types of FET device structures in which the ZnO nanowires are placed on the substrate or suspended above the substrate. The photoluminescence studies of the ZnO nanowires provide substantial evidence that the observed threshold voltage shift in nanowire transistors can be explained by a surface-band-bending through the gate electric field modulation, resulting from the irradiation-induced charges. Finally, as a practical approach, we demonstrate the logic inverter circuits made from the operation mode-controlled ZnO nanowire FETs.

Keywords: ZnO nanowires, field effect transistors, electronic properties, surface states, operation mode, proton irradiation, logic circuit

1. INTRODUCTION

Nanomaterials such as semiconducting nanowires or carbon nanotubes are promising nanobuilding blocks for nanoelectronic device applications. One of the key issues of nanomaterial-bsed device applications is the presence and significance of interfaces and interfacial states[1]. The interfaces can play an important role in electronic transport for conventional metal-oxide-semiconductor field effect transistors (MOSFETs), thin film transistors (TFTs), and especially nanowire transistors[1-3]. Thus, the unique interplay of all these interface properties has a profound effect in determining the function and performance of nanowire-based device. In addition, another key issue is controlling the electronic properties especially of the field effect transistors (FETs), which is very important for achieving or improving novel functionalities. To date, there have been considerable efforts to control the channel conductance and the threshold voltage (or operation voltage) for FETs, for example, impurity doping, attaching molecules, and changing surface or interface states in the active region were tried[4-6]. In particular, for the nanoscale FETs, controlling the threshold voltage is a major challenge for realizing the desired functions because nanowire FETs are the fundamental element for nanoelectronic device applications[7]. Therefore, it is essential to understand and control the influence of interface states on the electronic transport properties of nanowire transistors.

In this report, we demonstrated the influence of interface and/or surface structure on the electronic transport characteristics, the adjustment of operation voltage in ZnO nanowire transistors, and their logic circuit applications by fabricating surface-architecture-controlled ZnO nanowrie FETs and by proton irradiation engineering. ZnO nanowires have attracted considerable attention due to their direct wide band gap (~3.4 eV), large exciton binding energy (~60 meV), and potential use in versatile applications such as FETs, chemical and biological sensing, light-emitting devices, solar cells, and logic circuits[1,8,9]. In order to understand the influence of interface and/or surface states on the electrical behavior of ZnO nanowire FET devices and to control their threshold voltage, we synthesized the surface morphology- and size-controlled ZnO nanowires on various substrates and introduced the proton-irradiation-assisted manipulation. The synthesis of surface morphology-and size-controlled nanowires facilitates the fundamental study of nanoscale

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devices with unique electrical properties. Specifically, the electrical transport behavior of nanowire transistors can be strongly influenced by the surface states, which are closely related to the surface morphology and size of nanowires. Therefore, control of the density of surface states is a crucial factor in various device applications. Furthermore, the irradiation of high energetic charged particles can have beneficial effects providing devices with desired functionalities and it may be used to tailor the structural, mechanical, electronic, and even magnetic properties of nanomaterials for applications in nanoelectronics, energy, and nanobiotechnology[10].

2. EXPERIMENTAL METHODS

2. 1 Surface-architecture-controlled ZnO nanowires

ZnO nanowires with smooth and rough surface morphology were grown on ZnO buffer film-coated c-plane sapphire substrates with or without Au catalysts by a vapor transport method. The general growth method of ZnO nanowires has been reported in detail elsewhere[11]. For the growth of the surface morphology- and size-controlled ZnO nanowires, we used various substrates: (1) an undoped ZnO film with Au catalyst (denoted as Au−ZnO film) or without Au catalyst (denoted as ZnO film), (2) a gallium-doped ZnO film with Au catalyst (denoted as Au−GZO film) or without Au catalyst (denoted as GZO film), (3) an aluminum-doped ZnO film with Au catalyst (denoted as Au−AZO film) or without Au catalyst (denoted as AZO film), and (4) an Au-coated sapphire (denoted as Au−sapphire) substrate. The size, surface morphology, and crystal structure of the ZnO nanowires were characterized using field emission scanning electron microscopy (FESEM) and transmission electron microscopy (TEM). The optical properties of the ZnO nanowires at room temperature were characterized by the photoluminescence (PL) mapping system (RPM2000 model, Accent Opt. Tech., U.K.) with a 325 nm He−Cd laser as an excitation source. Note that in order to eliminate signals coming from the ZnO buffer films themselves, ZnO nanowires were transferred from the growth substrates to silicon wafers, and the PL spectra were obtained from the ZnO nanowires transferred on silicon wafers. In addition, in order to enable statistical analysis of the electrical transport behaviors of surface-architecture-controlled ZnO nanowires, a total of 327 nanowire FET devices were fabricated and characterized. A detailed description of the fabrication of ZnO nanowire FET devices has been reported elsewhere[11]. The electronic transport characteristics of the surface-architecture-controlled ZnO nanowire FETs were investigated using a semiconductor parameter analyzer (HP4155C) at room temperature.

As for the application toward logic circuits of smooth and rough nanowires, the logic inverters composed from two types of ZnO nanowires were fabricated[12]. Firstly, nanowires were selectively transferred to the substrate defined by photoresist. Then, Ti (30 nm)/Au (40 nm) source and drain electrodes were fabricated using photolithography and lift-off process. Cross-linked poly-4-vinylphenol (cPVP) was spin coated as a gate dielectric, followed by the deposition of an Al (50 nm) as top gate electrode. Finally, interconnected lines for logic inverters were patterned with a shadow mask. The current-voltage transfer characteristics of transistors and logic inverters were measured using a semiconductor parameter analyzer in an ambient atmosphere.

2.2 Proton irradiation-assisted manipulation

The Two types of FET devices, i.e., on-substrate-type devices where nanowires are placed on the substrate and suspended-type devices where nanowires are suspended above the substrate, were fabricated using ZnO nanowires. The growth method of ZnO nanowires and the fabrication method of on-substrate-type FET devices have been described in detail elsewhere[13]. All the fabricated on-substrate-type FETs were passivated by PMMA to minimize the influence of water or gas molecules on ZnO nanowire FETs and to enhance the gate-coupling effects[13]. The suspended-type FETs were fabricated in the following steps. First, a thin photoresistor (PR) layer was coated on a silicon substrate with 300 nm-thick SiO_2 using spin-coating at 8,000-10,000 rpm, followed by soft-baking. Then the suspension of ZnO nanowires was dropped onto the thin PR-coated substrates. A second thick PR layer was coated on the ZnO nanowire-dropped substrates by spin-coating at 4,000 rpm, followed by soft-baking. Finally, metal electrodes consisting of Ti (200 nm)/Au (200 nm) were defined as source and drain electrodes using the photolithography and lift-off process. Then, the fabricated suspended-type devices were irradiated by a proton beam.

For the proton irradiation experiments, accelerated proton beams of 10 MeV were generated using a MC-50 cyclotron (at the Korea Institute of Radiological and Medical Sciences). In our study, the total fluences (Φ) during proton irradiation were 10^{10}, 10^{11}, and 10^{12} cm^{-2}, corresponding to irradiation times of 60, 600, 6000 sec, respectively. The

electrical properties of both the on-substrate-type and suspended-type FETs were characterized systematically before and after proton irradiation using a semiconductor parameter analyzer (HP4155C) at room temperature. The optical properties of the ZnO nanowires before and after proton irradiation were studied by micro-photoluminescence (μPL) and temperature-dependent PL with a 325 nm He-Cd laser as an excitation source.

For applications of hybrid complementary logic circuits consisting of ZnO nanowire and single-walled carbon nanotube (SWNT)-network FET devices, a suspension of SWNTs (commercially available from Iljin Nanotech Co., Ltd., Korea) in 1,2-dichlorobenzene (o-DCB) (from Sigma–Aldrich) was prepared by a combination of sonication and centrifugation[14]. Fabrication processes of the hybrid complementary logic circuits have been described in detail elsewhere[14]. The current–voltage transfer characteristics of transistors and logic circuits were measured using a semiconductor parameter analyzer (Agilent B1500A). The evaluation of the AC electrical characteristics was performed using a pulse pattern generator (Agilent 81104A) and a digital oscilloscope (TDS 3054).

3. RESULTS AND DISCUSSION

3.1 Surface-architecture controlled ZnO nanowires

In order to study the electrical properties of surface-tailored ZnO nanowires, we fabricated the FET devices as a typical back-gated configuration. The representative transfer characteristics (I_{DS}-V_G) (at V_{DS} = 0.1 V) of the FETs made from the surface-architecture-controlled ZnO nanowire and their TEM images are shown in figure 1 and the insets, respectively. The nanowires grown on different substrates exhibited different electronic transport characteristics. The FET devices made from smooth ZnO nanowires grown on GZO and Au-AZO films and Au-sapphire substrate have negative threshold voltages, indicating n-channel depletion-mode (D-mode) behaviors that exhibit nonzero current at the zero gate bias.

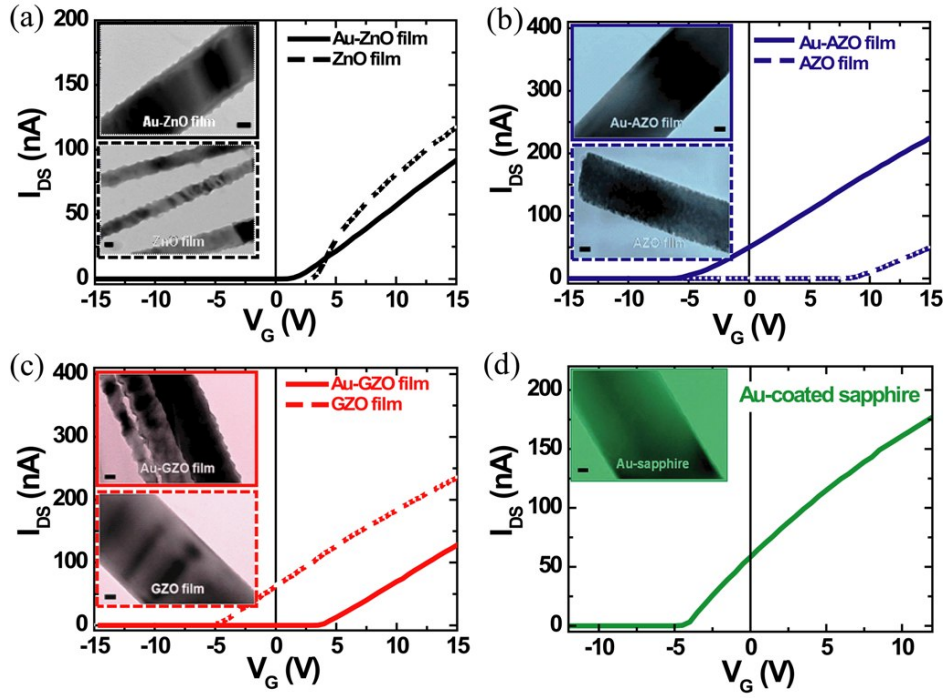

Figure 1. The transfer characteristics (I_{DS}-V_G) of FETs made from ZnO nanowires grown on various substrates, measured at V_{DS} = 0.1 V. The insets show TEM images of the ZnO nanowires grown on various substrates: (a) undoped ZnO film, (b) Al-doped ZnO film, (c) Ga-doped ZnO film with and without Au catalysts, and (d) Au-coated sapphire substrate, respectively. The scale bars are 20 nm.

In contrast, the FETs made from rough ZnO nanowires grown on Au-ZnO, ZnO, Au-GZO, and AZO films have positive threshold voltages, indicating n-channel enhancement-mode (E-mode) behaviors that exhibit off-current status at zero gate bias. The rough ZnO nanowires have relatively smaller diameters and positive threshold voltages, whereas smooth ZnO nanowires have relatively larger diameters and negative threshold voltages. The positive threshold voltage is attributed to deep traps in the channel or at the interface, whereas the negative threshold voltage is attributed to delocalized electrons from shallow donors in the channel[15]. This result indicates that the surface morphology and the nanowire size associated with surface states can have a significant influence on the operation mode of nanowire-based FET devices.

To provide substantial evidence that the observed two different transport behaviors in nanowire transistors can be attributed to the surface states and to study the corelation between the electrical and optical properties, the PL spectra were measured for ZnO nanowires grown on various substrates. As shown in figure 2(a), the PL emissions of the ZnO nanowires consist of two main bands; one is the ultraviolet (UV) emission band with a peak position between 375 and 380 nm. The other is the broad defect emission (or deep-level (DL) emission) in the visible range. The defect emission is determined by the surface states and/or the concentration of the corresponding surface defects[16,17]. Although both the smooth and rough types of ZnO nanowires have both UV and defect emission peaks, the UV-to-DL emission ratios (I_{UV}/I_{DL}) are very different between smooth and rough ZnO nanowires. Figure 2(b) shows the relationship between the I_{UV}/I_{DL} ratios of the PL spectra [obtained from figure 2(a)] and the nanowire diameter. The I_{UV}/I_{DL} ratios can be fitted with surface-recombination-layer approximation model as following[16],

$$\frac{I_{UV}}{I_{DL}} = C\left(\frac{(D/2)^2}{2(D/2)t - t^2} - 1\right) \tag{1}$$

where C is an approximation constant related to a collection efficiency difference at wavelengths of UV emission and defect emission peaks, D is the nanowire diameter, and t is a surface recombination thickness. The thickness of the surface recombination layer (t) was assumed to be 30 nm. The optimized fitting curve obtained with equation (1) (using t = 30 nm and C = 1.05) is plotted as the dashed line in figure 2(b). For the smooth ZnO nanowires with relatively larger diameters, the defect emission is weak and the UV emission becomes relatively strong, whereas for the rough ZnO nanowires with relatively smaller diameters, the defect emission is strong and the UV emission becomes relatively weak. This indicates that the ZnO nanowires with large I_{UV}/I_{DL} ratios have a low density of surface states, whereas those with small I_{UV}/I_{DL} ratios have a high density of surface states[16,17]. Interestingly, the luminescence of ZnO nanowires grown on various substrates is dependent on the surface morphology and the size of nanowires associated with surface states.

Figure 2(c) summarizes the temperature-dependent free exciton (FX) peak positions from low temperature PL spectra in the range of 10–300 K for two types of ZnO nanowires, which can be successfully described by Varshni's empirical formula, and the fits are plotted as solid lines through the data points. The energy position of the FX peak for the rough ZnO nanowires rapidly shifts to lower energy region with increasing temperature than for the smooth ZnO nanowires. This shift can be attributed to the influence of surface defects on excitonphonon interaction as well as laser-induced heating in nanostructure ensembles[18]. However, it is more likely that the surface defects greatly contribute to the observed peak shift. It is well known that the UV emission of ZnO nanostructures is commonly attributed to the direct recombination of excitons through an exciton-exciton scattering[18]. For our two types of ZnO nanowires, a FX, a neutral-donor-bound exciton, and their LO-phonon replicas are located at the same energy positions at low temperature (not shown here)[18]. In order to investigate the effects of surface defects on the exciton-LO-phonon interaction, the shape of each room-temperature PL spectrum was fitted using Lorentzian functions, which are a good approximation to determine the relative contribution of FX, FX-1LO (F1), and FX-2LO (F2) peaks as shown in the inset of figure 2(c). It can clearly be seen that the emission of both smooth and rough ZnO nanowires is composed of FX, F1, and F2 peaks merging into one broad peak. More interestingly, the relative contribution of the F1 line to the UV emission peak at room temperature is stronger in the rough ZnO nanowires than in the smooth ZnO nanowires, leading to a shift of the UV emission peak to lower energy region. These observations suggest that the crystal environment near surface in the rough ZnO nanowires is different from in the smooth ZnO nanowires. It has been known that in semiconductors with polarity and ionicity such as ZnO and GaN, the interaction between free excitons and LO-phonons can be mainly occurred by the Fröhlich interaction, which is a Coulomb interaction between electrons and the longitudinal electric field produced by the LO-phonons[18]. In particular, the first order phonon-assisted free exciton emission (FX-1LO) in the Fröhlich interaction is vanishingly small for a perfect crystal due to parity conservation[18]. However, since the Fröhlich interaction can be mainly influenced by the incorporation of defects in a crystal, the strength of exciton-phonon coupling can be remarkably changed[18]. Therefore, we believe that the strong contribution of F1 line for the rough ZnO NWs is attributed to a high

density of surface defects associated with the rough surface of ZnO nanowires. In addition, figure 2(d) shows the PL contour plots of temperature-dependent defect emissions of two types of ZnO nanowires. A relatively strong defect emission of the rough ZnO nanowires indicates that the rough ZnO nanowires have a significantly greater number of surface defects[17,18]. Consequently, these surface states of ZnO materials introduce various defect energy levels inside the band gap of ZnO[17,18], so that the surface effects by such surface states influence the ZnO nanowire-based devices as shown in figure 1.

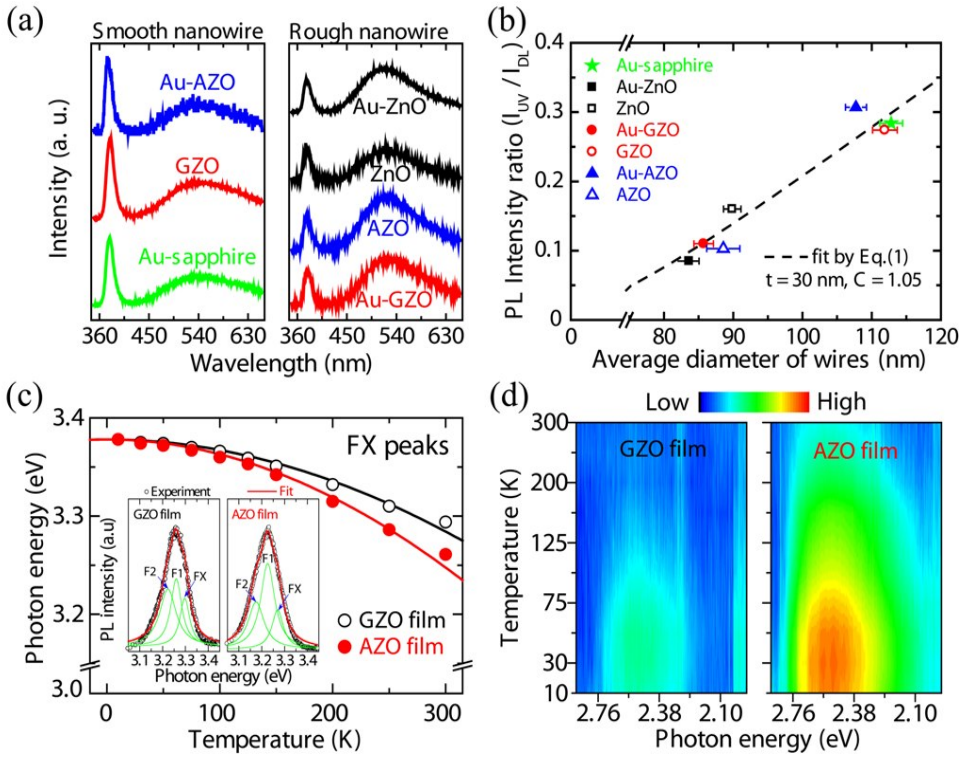

Figure 2. (a) PL spectra of the ZnO nanowires grown on various substrates. (b) PL intensity ratios I_{UV}/I_{DL} with a fitting curve as a function of the average diameter of ZnO nanowires. (c) Temperature dependence of free exciton (FX) peak position. The solid lines are the fitting curves of the experimental data by Varshni's formula. Lorentzian curves for the room-temperature UV emissions showing the contributions from the FX, F1, and F2 emission curves. The sums of the three Lorentzians are indicated by the solid curves (red). (d) PL contour plot of temperature-dependent defect emissions.

Now, we can explain the mechanism of different operation modes in relation with surface states. Figure 3 shows the cross-sectional schematics (top figures) across the electrodes, ZnO nanowire, and dielectric layers with the corresponding equilibrium energy band diagram (bottom figures) of the ZnO nanowire FETs at $V_G = 0$ V. Figure 3(a) shows the case for smooth ZnO nanowire FETs, and figure 3(b) shows the case for rough ZnO nanowire FETs. The surface states on single crystalline nanowires can act as trap sites at the interfaces, resulting in surface band bending due to Fermi level pinning[11,19]. The carrier trap states at the interfaces are important in determining the operation modes of transistors[15,19]. The trapping of carrier electrons in the trap states can cause electron depletion in the channel, resulting in a gate threshold voltage shift and a conductance modulation. In particular, rough ZnO nanowires with relatively smaller diameters can have a more significant fraction of the surface depletion region in the nanowire channel due to electron traps in comparison with smooth ZnO nanowires. As a result, the smooth ZnO nanowire FETs with relatively larger diameters can operate in the n-channel depletion-mode behavior with a partially depleted channel region [figure 3(a)], whereas the rough ZnO nanowire FETs with relatively smaller diameters can operate in the n-channel enhancement-mode behavior with a fully depleted channel region [figure 3(b)] under the no-gate-bias condition.

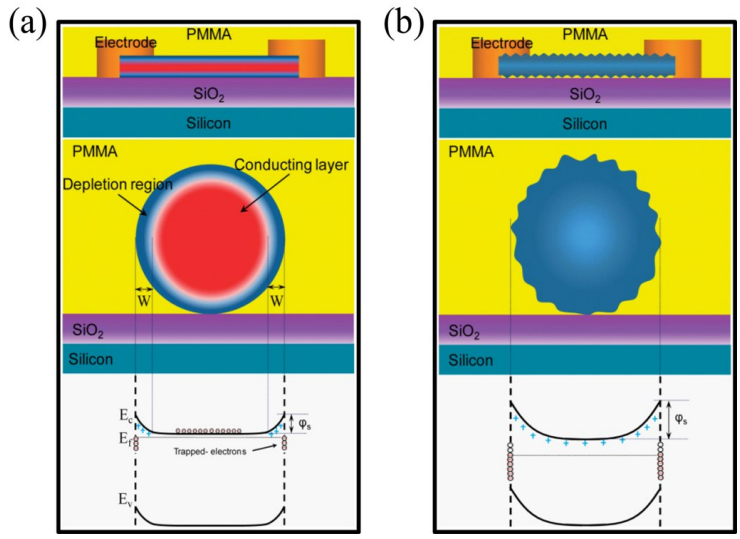

Figure 3. (Top) Cross-sectional schematics across the electrodes, ZnO nanowire, and dielectric layers, and (bottom) the corresponding equilibrium energy band diagrams of nanowire FETs at V_G = 0 V for (a) smooth and (b) rough ZnO nanowires.

For wide application of nanowire FET-based logic circuits with a simple circuit design and high logic performance, both depletion mode and enhancement mode FETs are often required[12]. Accordingly, we fabricated the logic inverter circuit constructed from a combination of both depletion mode and enhancement mode nanowire FETs [figure 4(a)]. Figure 4(a) shows the schematic structure of a logic inverter that uses a depletion mode FET made from the smooth ZnO nanowires and an enhancement mode FET made from the rough ZnO nanowires. Figure 4(b) shows the typical voltage

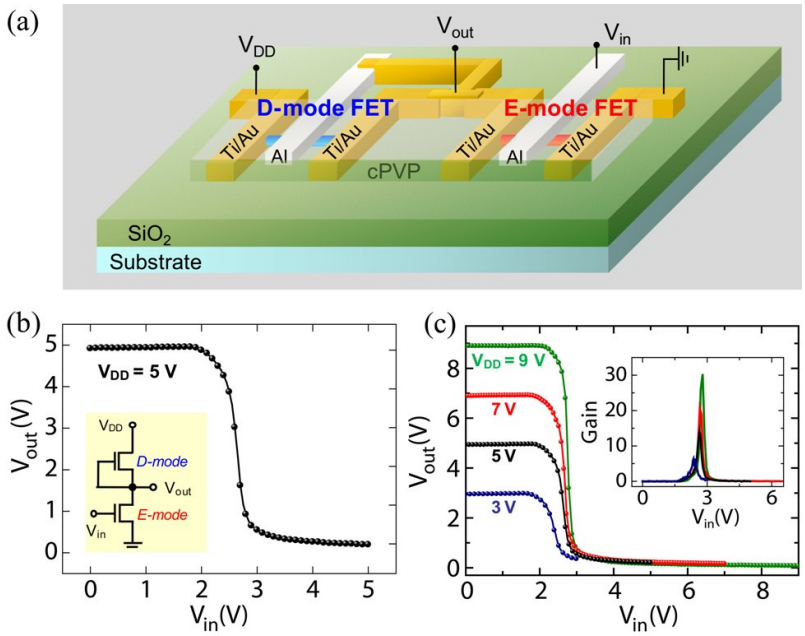

Figure 4. (a) Schematic illustration of logic inverter composed of D-mode and E-mode nanowire FETs. (b) VTC curve of a logic inverter composed of n-channel D-mode and n-channel E-mode ZnO nanowire FETs, obtained at V_{DD} = 5 V. The inset shows an inverter circuit diagram. (c) VTC curves of the inverter obtained at V_{DD} = 3, 5, 7, 9 V. The inset shows voltage gain curves derived from the various VTC curves.

transfer characteristic (VTC) of a logic inverter made from two types of ZnO nanowire FETs operating under a supply voltage (V_{DD}) of 5 V. In the circuit diagram of the inverter circuit (inset of figure 4(b)), the n-channel D-mode nanowire FET is a load device and the n-channel E-mode nanowire FET is a driver device. The inverter response to stage switching was clearly observed in the input voltage (V_{in}) range from low (0 V) to high (5 V), displaying its transition voltage (V_T) of ~2.6 V. Furthermore, the gain ($-dV_{out}/dV_{in}$) of our inverter circuit is ~14, with well-matched noise margins of 1.9 V and 2.0 V. Figure 4(c) shows VTCs of the inverter for various supply voltages (V_{DD}) from 3 to 9 V with a step of 2 V. The inverter gains appear to increase with an increase in supply voltage, ranging from 6.4 to 30.3 (inset of figure 4(c)). Higher gain means that the high to low logic transition is much sharper, from which one can expect a more acceptable logic operation for high speed circuit application[12]. Furthermore, as V_{DD} is increased, the resistance of the driver (E-mode FET) becomes smaller than that of the load device (D-mode FET).

3.2 Proton irradiation-assisted manipulation

Two types of FET devices, an on-substrate type where nanowires are placed on the substrate and a suspended type where nanowires are suspended above the substrate, were fabricated using single-crystal ZnO nanowires grown by the vapor transport method. The proton irradiation of two types of FET devices is schematically illustrated (top) in figure 5, which also shows SEM images (bottom) of fabricated devices. The electrical characteristics of the on-substrate-type FETs are summarized in figure 6. Figure 6 shows the representative data of the output characteristics (I_{DS}-V_{DS}) and transfer characteristics (I_{DS}-V_G) before and after proton irradiation with fluences of 10^{10} cm^{-2} [figure 6(a)], 10^{11} cm^{-2} [figure 6(b)], and 10^{12} cm^{-2} [figure 6(c)], respectively. The I_{DS}-V_{DS} curves have well-defined linear regimes at low biases and saturation regimes at high biases both before and after proton irradiation, indicating typical pinch-off characteristics of n-type semiconductor FETs. A interesting finding in the I_{DS}-V_{DS} curves is that the electrical conductance increased after a short irradiation time ($\Phi = 10^{10}$ cm^{-2} corresponding to an irradiation time of 60 sec) under the same applied gate bias conditions, whereas after long irradiation times ($\Phi = 10^{11}$ cm^{-2} corresponding to 600 sec and $\Phi = 10^{12}$ cm^{-2} corresponding to 6000 sec), the electrical conductance decreased. Moreover, the I_{DS}-V_G curves reveal that the on-substrate-type FET exhibits a negative threshold voltage shift after a short irradiation time, whereas the device displays a positive threshold voltage shift after a long irradiation time.

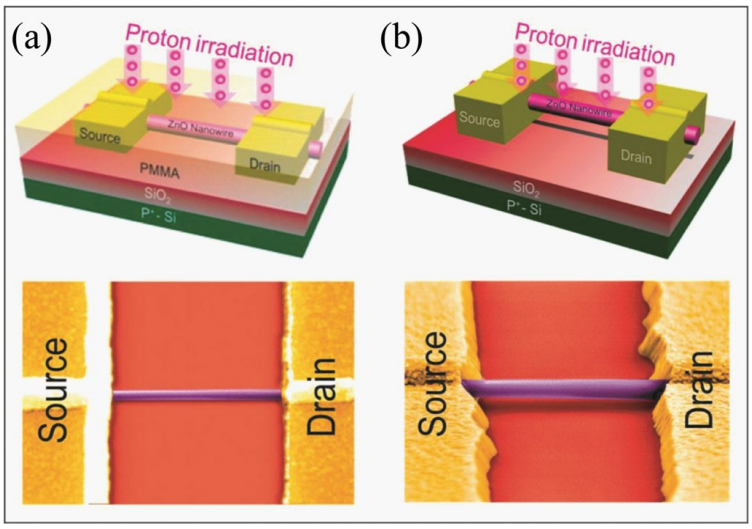

Figure 5. Schematic views (top) and SEM images (bottom) of (a) the on-substrate-type and (b) the suspended-type ZnO nanowire FETs.

High-energy proton irradiation can generate electron-hole pairs in SiO_2, resulting in irradiation-induced charges, i.e., positive oxide-trapped charges (or positive oxide traps, Q_{ot}) and negative interface states (or interface traps, D_{it})[13]. The generation of such charges can play a key role in the controllable tuning of the electrical properties of ZnO nanowires. For the on-substrate-type FETs, the positive oxide traps and negative interface traps have a significant

influence on the surface depletion and carrier concentration in the ZnO nanowire channel, which is responsible for the tuning of the operation voltage as well as the modulation of the electrical conductance. Specifically, the positive oxide traps in the bulk SiO_2 layer act as an enhancement of the gate electric field, resulting in an increased carrier concentration and a negative threshold voltage shift. On the other hand, the negative interface traps increase the surface depletion region, resulting in a reduction of carrier concentration and a positive threshold voltage shift. Therefore, the observed threshold voltage shift of on-substrate-type FETs after proton irradiation can be explained by the combination effects of oxide traps and interface states[13].

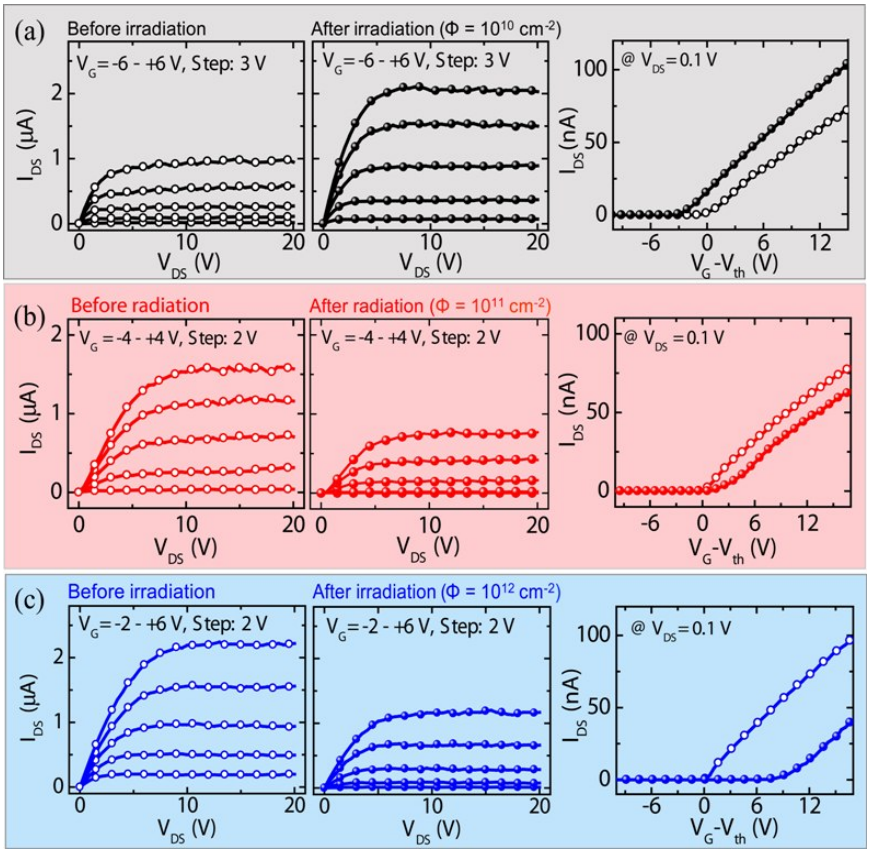

Figure 6. Electrical characteristics before (open circles) and after (filled circles) proton irradiation at an energy of 10 MeV with fluences of (a) 10^{10} cm^{-2} (corresponding to an irradiation time of 60 s), (b) 10^{11} cm^{-2} (corresponding to an irradiation time of 600 s), and (c) 10^{12} cm^{-2} (corresponding to an irradiation time of 6000 s).

To provide substantial evidence that the observed threshold voltage shift in the on-substrate-type FETs can really be attributed to two different types of irradiation-induced charges, and in particular to unambiguously explain the effect of irradiation-induced interface states at the SiO_2/ZnO nanowire interface, we fabricated a suspended-type FET device structure, which has no effect by the interface states at the SiO_2/ZnO nanowire interface. In addition, we further investigated whether the ZnO nanowire itself was affected or not by the proton irradiation using micro-photoluminescence (μPL) and temperature-dependent PL measurements. The electrical properties of the suspended-type devices before and after proton irradiation are summarized in figures 7(a)-7(c). All of the I_{DS}-V_{DS} curves before and after irradiation show almost linear characteristics, indicating a good ohmic contact. Notably, the suspended-type FET devices have a relatively weaker gating effect in the gate voltage range between -10 and +10 V due to the suspended geometry. Interestingly, unlike the case for on-substrate-type devices (figure 6), the current-voltage characteristics (I_{DS}-V_{DS}) at various gate biases in the suspended-type devices [figures 7(a)-7(c)] show an increase in the electrical conductance due to proton irradiation effects for both short and long irradiation times. As discussed earlier, this observation can be explained by the existence of only irradiation-induced positive oxide traps without the interface-state effect, resulting in

an enhancement of the gate electric field in the suspended-type device structure. In other words, the increased conductance at the same applied gate bias after irradiation exhibits an increased carrier concentration induced by an enhancement of the gate electric field due to positive oxide trpas in this type of device structure.

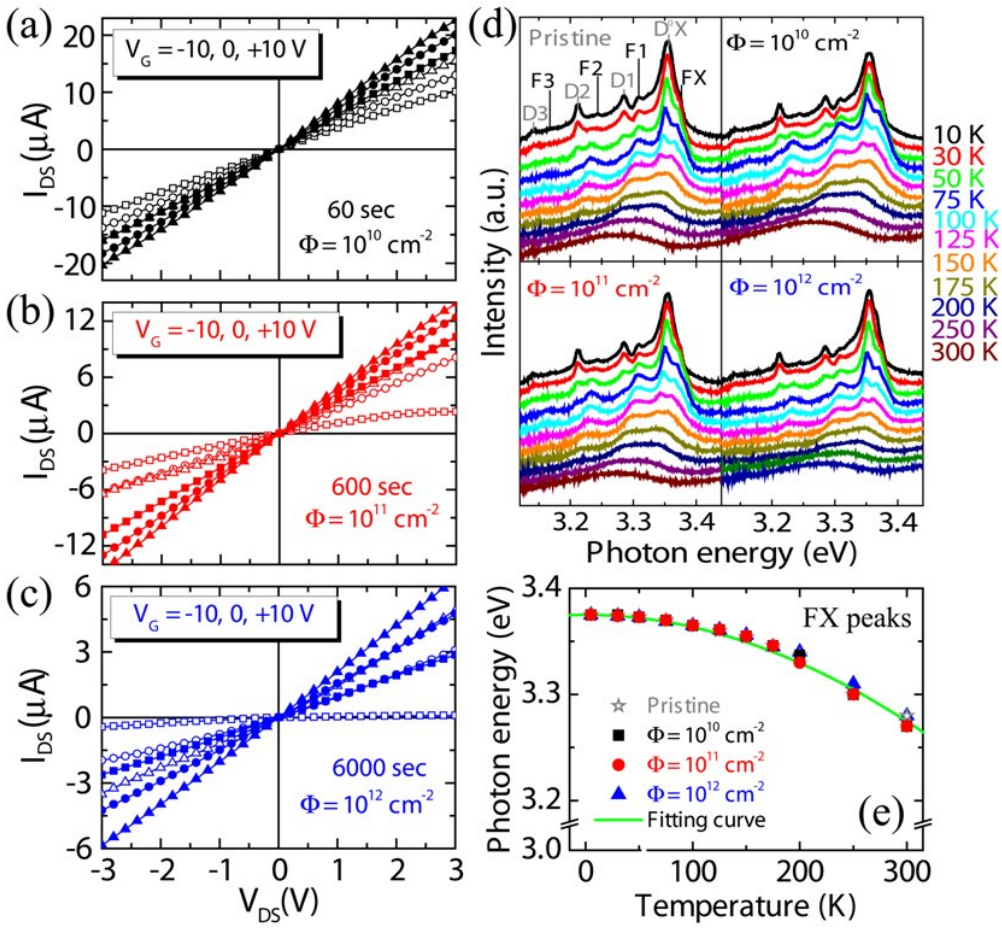

Figure 7. The output characteristics (I_{DS}-V_{DS}) with various gate bias voltages (V_G = -10, 0, +10 V) before (open symbols) and after (filled symbols) proton irradiation at an energy of 10 MeV with fluences of (a) 10^{10} cm^{-2} (60 s), (b) 10^{11} cm^{-2} (600 s), and (c) 10^{12} cm^{-2} (6000 s). (d) Temperature-dependent PL spectra, showing the excitons and their LO-phonon replicas for the pristine and proton-irradiated ZnO nanowires. (e) Temperature dependence of FX peak position. The solid line is a fitting curve of the experimental data by Varshni's formula.

Figures 7(d) and 7(e) show the temperature-dependent PL spectra of ZnO nanowires in the temperature range of 10-300 K. It is well known that the PL spectra of ZnO nanostructures is commonly attributed to the direct recombination of excitons through an exciton–exciton scattering[20]. Here, we have found that the PL characteristics originate mainly from the recombination of free exciton (FX) and donor bound exciton (D^0X) since a free exciton (FX), a neutral-donor-bound exciton (D^0X), and their longitudinal optical (LO) phonon replicas, which are located at the same energy positions at low temperature, are clearly seen in figure 7(d). The LO-phonon replicas of FX and D^0X are labeled FX-1LO (F1), FX-2LO (F2), FX-3LO (F3), D^0X-1LO (D1), D^0X-2LO (D2), and D^0X-3LO (D3)[13]. Their LO-phonon replicas are observed with a separation of ~72 meV, which corresponds to the LO-phonon energy of ZnO[13]. The exciton emission shifts to lower energy with increasing temperature due to thermal activation of carriersS6 and the FX and its LO-phonon replicas become stronger in intensity relative to the D^0X-related peak. In addition, as temperature increases, the D^0X-related emissions decrease more rapidly than the FX-related emissions due to thermal dissociation of the donor-bound-related excitons, and thus the FX-related emission remain at room temperature. All these results indicate that for the

pristine and proton-irradiated ZnO nanowires, D^0X-related transitions are dominant at low temperature, whereas FX-related transitions are dominant at high temperature. Figure 7(e) shows the temperature-dependent FX peak positions in the temperature range of 10-300 K for the pristine and proton-irradiated ZnO nanowires. The temperature dependence of the FX transition energy can be expressed by Varshni's empirical formula[13]. It can be clearly seen that the peak positions of FX for the proton-irradiated ZnO nanowires do not change with respect to those for the pristine ZnO nanowires, indicative of irradiation hardness of the ZnO nanowires themselves[13,21]. Therefore, the proton irradiation effect on the ZnO nanowire FET devices is due to the irradiationinduced charges in the bulk SiO_2 layer and at the SiO_2/ZnO nanowire interface, but not by the ZnO nanowires themselves.

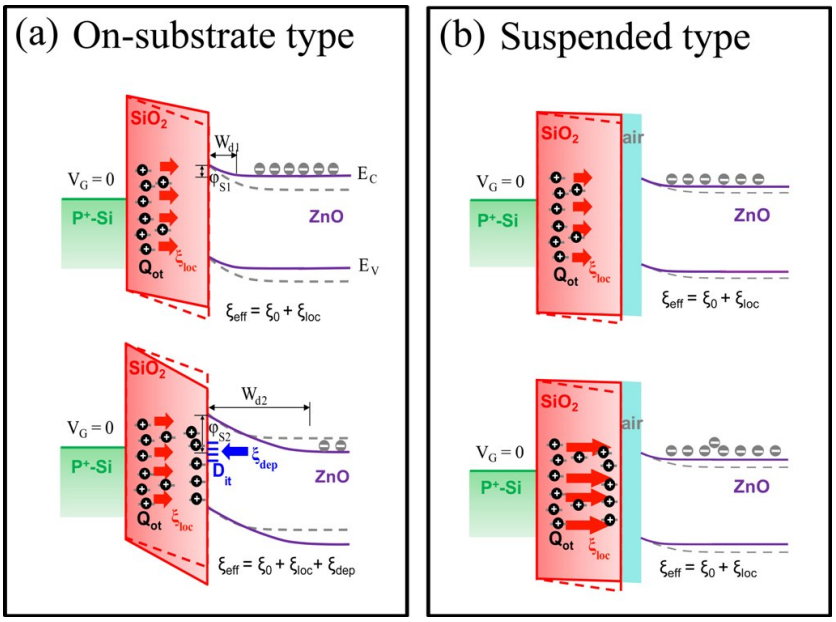

Figure 8. Energy band diagrams of (a) the on-substrate-type and (b) the suspended-type ZnO nanowire FETs before and after a short irradiation time (top) and a long irradiation time (bottom). The red and blue arrows indicate the electric field modulation due to proton irradiation-induced charges (see text for details).

Here, the experimental observations of the proton beam irradiation effects on the two types of device structures studied are explicitly explained using a surface-band-bending model, as shown in figure 8. Figures 8(a) and 8(b) show the equilibrium energy band diagrams at $V_G = 0$ V before and after proton irradiation of the on-substrate-type and suspended-type FET devices, respectively. For the on-substrate-type FET device after a short irradiation time [figure 8(a), top], the electronic conduction (E_C) and valence (E_V) bands of ZnO show surface-band-bending with a smaller surface depletion width (W_{d1}) and a relatively lower surface barrier potential (φ_{S1}) at the SiO_2/ZnO nanowire interface, resulting from an enhancement of the gate electric field due to the positive oxide traps (Q_{ot}) in the bulk SiO_2. Conversely, the electronic bands observed after a long irradiation time [figure 8(a), bottom] show surface-band-bending with a relatively larger surface depletion width (W_{d2}) and higher surface barrier potential (φ_{S2}), resulting from the formation of a destructive electric field due to the negative interface traps (D_{it}). In other words, for the case of long irradiation times, a strong electric field (ξ_{dep}) exists in an extended surface depletion region due to increased surface-band-bending by the interface states[13,22]. The effective gate electric field experienced by the carriers in the channel, taking into consideration the cylindrical nanowire channel geometry, can be estimated using the following equations[13,23],

$$\xi_{eff} = \frac{1}{\varepsilon_{ZnO}}\left(\frac{1}{2}Q_{tot} + Q_d\right) \tag{2}$$

and

$$Q_d = -q\,N_d\,W_d = -\sqrt{2\varepsilon_{ZnO}\,qN_d\,\varphi_s} \tag{3}$$

where ξ_{eff} is the effective gate electric field, ε_{ZnO} is the ZnO permittivity (8.66), Q_{tot} is the total charge density in the ZnO channel, Q_d is the depletion charge density in the ZnO channel, N_d is the doping density, W_d is the depletion region width, and φ_s is the surface barrier potential[13]. The effective gate electric field, ξ_{eff}, can be considered in terms of the initial field (ξ_0) before proton irradiation, the local electric field (ξ_{loc}), and the surface depletion electric field (ξ_{dep}) after irradiation. For the convenience of our discussion, assuming that ξ_{dep} before and after a short irradiation time is much weaker than that after a long irradiation time, ξ_{eff} can be expressed as a combination of ξ_0 and ξ_{loc} in the case of a short irradiation time, whereas in the case of a long irradiation time, ξ_{eff} is expressed as a combination of ξ_0, ξ_{loc}, and ξ_{dep}. Consequently, the electrical characteristics of the on-substrate-type FETs after a short irradiation time exhibit a negative threshold voltage shift and an electrical conductance increase due to the relatively higher effective gate electric field ($\xi_{eff,before} < \xi_{eff,after}$) under the same gate bias, whereas those after a long irradiation time exhibit a positive shift and a conductance decrease due to the lower effective gate electric field ($\xi_{eff,before} > \xi_{eff,after}$). On the other hand, for the case of the suspended-type FETs, since there is no ξ_{dep} due to the absence of irradiation-induced interface states, ξ_{eff} is always higher than that before irradiation ($\xi_{eff,before} < \xi_{eff,after}$). Thus, the electrical characteristics of the suspended-type FETs can exhibit an electrical conductance increase after both short and long irradiation times.

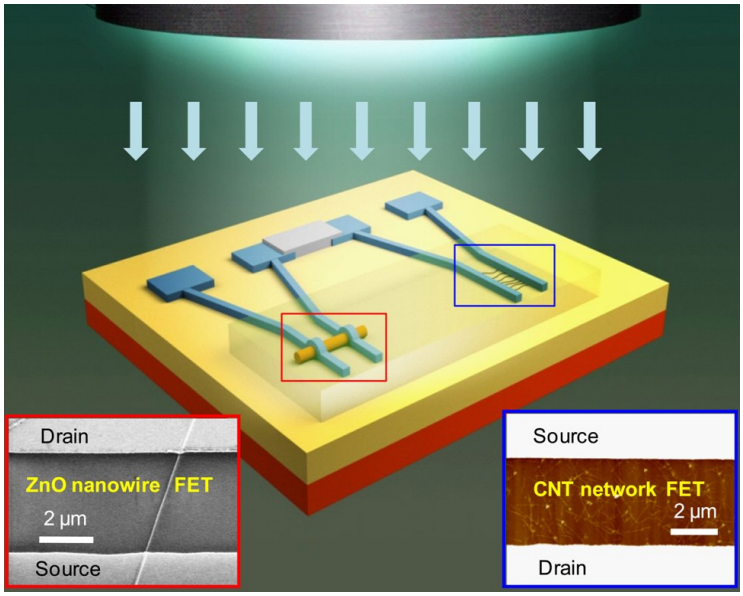

Figure 9. Device layout of the hybrid complementary logic circuit comprising n-channel ZnO nanowire and p-channel SWNT-network FET devices. The insets show atomic force microscopy image of an SWNT-network FET (right bottom) and field-emission scanning electron microscopy image of a ZnO-nanowire FET (left bottom).

The modulation of electrical conductance and threshold voltage by proton radiation is significantly important for logic circuit applications with less power consumption and the desirable switching behavior[14]. Accordingly, as a practical approach to the device applications based on the understanding and results on controllable tuning of the electronic properties of ZnO nanowire FETs by proton irradiation, hybrid complementary logic inverters using p-type single-walled carbon nanotube (SWNT) network FETs and n-type ZnO nanowire FETs before and after proton irradiation was fabricated and measured systematically[14,24]. Note that for the better and more practical circuit applications, it is significantly important to match the threshold voltage of both n- and pchannel transistors for favorable logic operation in circuits. Figure 9 shows the layout of an inverter device comprising p-type SWNT network (the inset of figure 9, right bottom) and n-type ZnO nanowire FETs (the inset of figure 9, left bottom). Figures 10(a) - 10(d) show the output characteristics and transfer characteristics of the n-channel ZnO nanowire and p-channel SWNT FETs, respectively, before and after proton irradiation with a fluence of 10^{11} cm^{-2}. Interestingly, the p-channel SWNT-network FET devices, showing no significant change in the electrical properties after proton radiation exposure [figures 10(c) and 10(d)], are highly resistant against proton beams[14,24], and have much less influence on surface-potential changes induced by the trap states formed at the CNT/SiO_2 interface[25].

As shown in figures 10(a)-10(d), we adjusted the threshold voltage of hybrid FETs through proton radiation to allow only electron and hole conductance for positive and negative gate bias, respectively. The inverter, showing desirable switching characteristics and a higher inverter gain, was constructed by adjustment of the threshold voltage of the ZnO-nanowire FETs with proton beam irradiations (10^{11} cm^{-2} and 10^{12} cm^{-2}), as shown in figures 10(e) and 10(f), respectively. Before proton radiation, the output voltage (V_{OUT}) of inverter varies from 5 V to 0 V as the input voltage (V_{IN}) varies from -2.5 V) to 2.5 V. These transfer characteristics of input–output voltage are deviated from the ideal operation of an inverter, which would have V_{IN} range of 0 – 5V with a switching voltage ($V_{IN} = V_{OUT}$) at 2.5 V. Thus, in order to avoid this voltage-transfer characteristic (VTC) problem, it is required to add an extra level-shifting element in a circuit design, but rendering it complicated and resulting in more power consumption[14]. Our hybrid logic inverter circuit is simple in circuit configuration and presents less operating-power consumption with the absence of an additional level shifter. Also, the VTC of our inverter circuit shows high noise margin and high inverter gain with full swing characteristics and less static power dissipation than single-carrier type-based circuits[14].

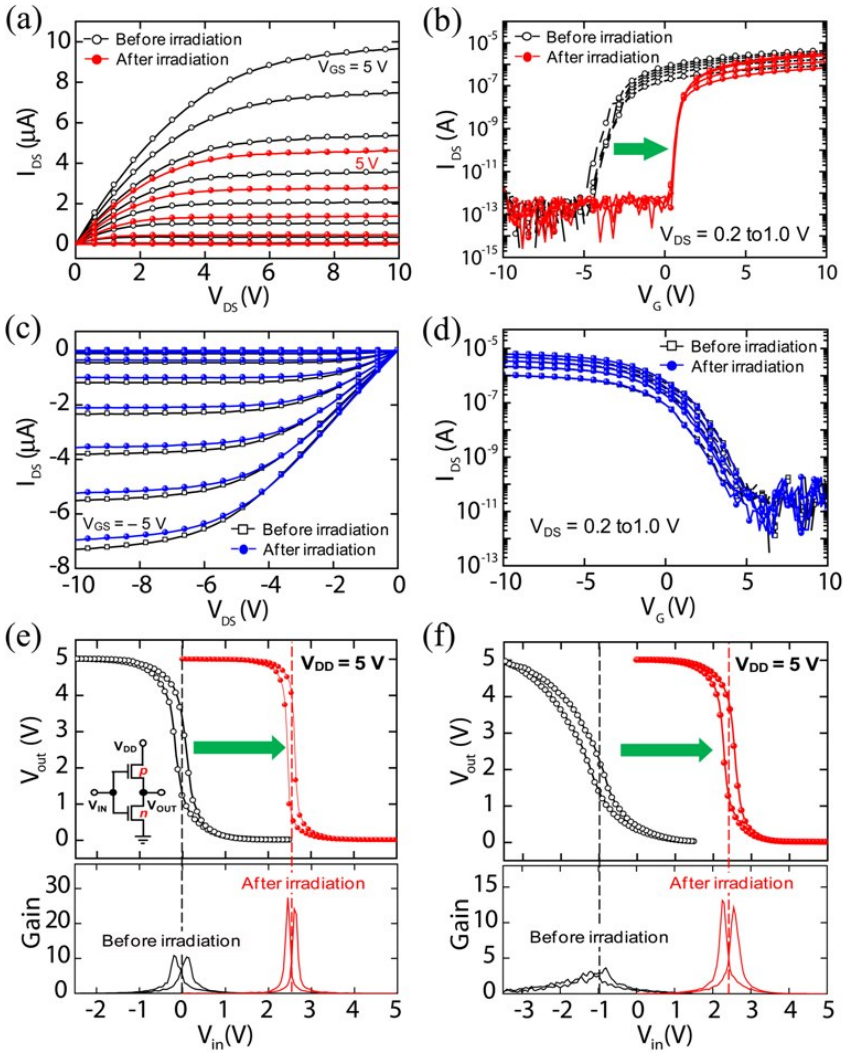

Figure 10. The electrical characteristics of a ZnO-nanowire FET and an SWNT-network FET before (open symbols) and after (filled symbols) proton irradiation: (a, c) the output characteristics (I_{DS}–V_{DS}) for various V_G from 1 to 5 V with a step of 1 V, and (b, d) the transfer characteristics (I_{DS}–V_G) for various V_{DS} from 0.2 to 1 V with a step of 0.2 V. (e, f) VTCs of a complementary inverter with changes in the switching voltage and inverter gain before (open symbols) and after (filled symbols) proton irradiations of 10^{11} cm^{-2} (e) and 10^{12} cm^{-2} (f). The VTCs show output voltage and gain as a function of input voltage for supply voltage (V_{DD} = 5 V). The inset of (e) shows the circuit schematic of the inverter.

4. CONCLUSIONS

In summary, it has been shown that surface states can be controlled by altering the surface-architecture of the ZnO nanowires grown on various ZnO buffer film-coated sapphire substrates through the vapor transport method. The surface-architecture-controlled ZnO nanowire FETs exhibited the surface morphology- and size-dependent electrical and optical properties. The FETs made from smooth ZnO nanowires with relatively larger diameters exhibited the n-channel depletion-mode behavior, whereas the FETs made from rough ZnO nanowire with relatively smaller diameters exhibited the n-channel enhancement-mode behavior. Furthermore, the ZnO nanowire logic inverter, which is composed of n-channel depletion-mode and enhancement-mode ZnO nanowire FETs with a polymer dielectric layer, has been demonstrated.

In addition, two types (on-substrate and suspended) of ZnO nanowire FET devices were fabricated and systematically characterized before and after the proton irradiation. The electrical characteristics of the on-substrate-type FETs demonstrated that the threshold voltage shift and electrical conductance can be modulated controllably by proton-irradiation-induced charges (positive oxide traps and negative interface traps). The electrical characteristics of the suspended type devices and PL studies provided substantial evidence that the threshold voltage shift and the electrical conductance modulation are due to the gate electric field modulation, resulting from the irradiation-induced charges. Lastly, we demonstrated hybrid logic inverters, which are composed of p-channel SWNT network and n-channel ZnO nanowire FETs, with the desirable switching characteristics by the adjustment of operation voltage through the proton irradiation in ZnO nanowire FETs. This proton irradiation-assisted manipulation can be a potentially useful way to create property-tailored nanoscale devices for developing their practical electronic devices.

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