Electrical properties of ZnO nanowire field effect transistors with varying high-*k* Al_2O_3 dielectric thickness

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We investigated the electronic properties of ZnO nanowire combined with the scaled high-*k* Al_2O_3 dielectrics using metal-oxide-semiconductor and field effect transistor (FET) device structures. We found that Al_2O_3 dielectric material can significantly reduce leakage currents when the applied voltage was restricted less than the transition voltage of direct tunneling to Fowler–Nordheim tunneling. The ZnO nanowire FETs with Al_2O_3 dielectrics exhibited the increase in electrical conductance, transconductance, and mobility and the threshold voltage shifted to the negative gate bias direction with decreasing Al_2O_3 dielectric layer thickness. © *2010 American Institute of Physics*. [doi:10.1063/1.3298910]

I. INTRODUCTION

Continuous miniaturization, such as physical channel length and gate dielectric thickness down to the nanometer scale, is becoming increasingly difficult in semiconductor technology due to limitations of fundamental physics such as tunneling leakage problem of ultrathin gate oxides used in metal-oxide-semiconductor (MOS) transistors.[1–5] To overcome this unavoidable problems, new device structures and material approaches have been proposed. For example, field effect transistors (FETs) based on nanowires and carbon nanotubes have been intensively investigated. These one-dimensional nanostructures have provided new challenges in terms of the controlled growth of nanoscale wire diameter and patterning processes at the nanometer scale.[6] In addition, the high-*k* dielectric materials including Al_2O_3, Y_2O_3, ZrO_2, and HfO_2 have been attractive due to its good surface adhesion, high capacitance, and thermal and chemical stability while reducing direct-tunneling leakage currents.[2–5]

In particular, the FET devices using nanostructures have been investigated using bottom-gate structure with a SiO_2 dielectric layer. However, as the SiO_2 dielectrics become thinner, the leakage current increases dramatically due to the quantum-mechanical tunneling effect through the dielectric layer.[5,7] Therefore, recently, the electrical properties of FETs based on semiconductor nanowires and carbon nanotubes combined with high-*k* gate dielectrics have been investigated.[8,9] For example, Javey *et al.*[8] reported integrating high-*k* dielectrics into carbon-nanotube transistors, which exhibited high transconductance and mobility without serious gate leakage current. And, logic circuits were successfully demonstrated using ZnO nanowire FETs with high-*k* dielectrics.[9]

Since a reduction in channel length accompanies diminishing oxide dielectric thickness, nanowire or nanotube FETs with high-*k* dielectrics are of great interest for potentially shrinking the device structures. Particularly, the leakage characteristics need to be thoroughly analyzed in a wide range of voltage, both below and above the transition voltage at which the leakage conduction is changed from direct tunneling (DT) to Fowler–Nordheim (FN) (or called as field emission) tunneling. In this work, we report on the electrical characteristics of ZnO nanowire FETs with Al_2O_3 dielectric layers. We have characterized the tunneling leakage current of the Al_2O_3 layers with different thickness in terms of the tunneling conduction mechanisms, and have investigated the electrical properties of the ZnO nanowire FETs with scaled Al_2O_3 dielectric layer.

II. EXPERIMENTAL SECTION

A. Fabrication of MOS structure with Al_2O_3 dielectric layer

The high-*k* Al_2O_3 layer used in this study was deposited by atomic layer deposition onto two types of substrates; a *p*-type silicon substrate and a heavily doped *p*-type silicon substrate. The *p*-type silicon substrate was used to fabricate the MOS structure [see inset of Fig. 1(a)] for extracting the dielectric constant of Al_2O_3 layer, whereas the heavily doped *p*-type silicon substrate was used to analyze tunneling characteristics of Al_2O_3 layer and to fabricate ZnO nanowire FETs. The Al_2O_3 layer was intended to grow to 20, 50, and

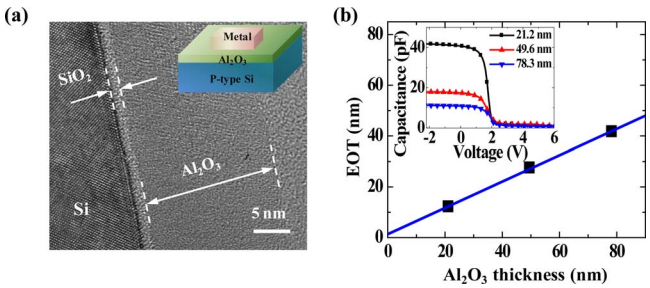

FIG. 1. (Color online) (a) HRTEM image of Al_2O_3 dielectric layer (21.2 nm). The inset shows schematic of a MOS device structure. (b) EOT vs thickness of Al_2O_3 dielectric layer. The inset shows a series of C-V characteristics.

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80 nm thick, but the actual physical thickness of Al_2O_3 layer was found to be ~19.7, 48.1, and 76.8 nm, respectively, when measured with a variable angle spectroscopic ellipsometer.

To reduce the oxygen vacancy in Al_2O_3 layer, the post deposition annealing (PDA) was carried out at 800 °C for 1 min at oxygen ambient. The PDA process was meant to enhance the stoichiometry of Al_2O_3 by reducing the oxygen vacancy and thus reducing the trap-assisted leakage currents.[10] An interfacial SiO_2 layer was also formed during the PDA process. The thickness of this interfacial SiO_2 layer was estimated as ~1.54 nm from the high resolution transmission electron microscopy (HRTEM) image in Fig. 1(a). Henceforth we refer to the Al_2O_3 layer thickness as the sum of the deposited Al_2O_3 layer and the interfacial SiO_2 layer thickness (~21.2, 49.6, and 78.3 nm). This interfacial SiO_2 layer can be formed naturally in the ambient air, and also can be formed by oxygen in the Al_2O_3 layer during the PDA process.[11]

After PDA process, metal electrode layers were deposited by an electron beam evaporator and defined as the junction electrode by using a photolithography and lift-off process. The capacitance-voltage (C-V) was measured by the MOS devices at 1.0 MHz frequency conditions at room temperature with Al_2O_3 dielectric layers grown on a *p*-type silicon. And, the leakage current-voltage was measured by the MOS devices with Al_2O_3 and SiO_2 dielectric layers grown on a heavily doped *p*-type silicon substrate using a semiconductor parameter analyzer (Agilent B1500A).

B. Fabrication of ZnO nanowire field effect transistors

We investigated the electrical properties of ZnO nanowire FETs with Al_2O_3 dielectric layers with the same three different thicknesses (21.2, 49.6, and 78.3 nm) as the MOS structure devices. For this purpose, the ZnO nanowires were grown via a vapor transport method on *c*-plane sapphire substrate coated with a thin Au film which acts as a catalyst for ZnO nanowire growth. The diameters of the ZnO nanowires were found to be 100.4 ± 12.2 nm, statistically determined from the field emission scanning electron microscopy (FESEM) images of ~100 different nanowires. This ZnO nanowire synthesis method has been explained in detail elsewhere.[12]

To fabricate ZnO nanowire FETs, the grown ZnO nanowires were transferred to Al_2O_3/Si (heavily doped *p*-type) substrate from the sapphire substrate. The heavily doped *p*-type silicon substrate acts as a back-gate electrode [see Fig. 2(a)]. Then source and drain electrodes (gap of 3–4 μm) are formed by using photolithography and lift-off process [see Fig. 2(b)]. The current-voltage characteristics of the ZnO nanowire FETs were measured using a semiconductor parameter analyzer (Agilent B1500A) at room temperature and restricted in a voltage range less than 3 V due to the FN tunneling current.

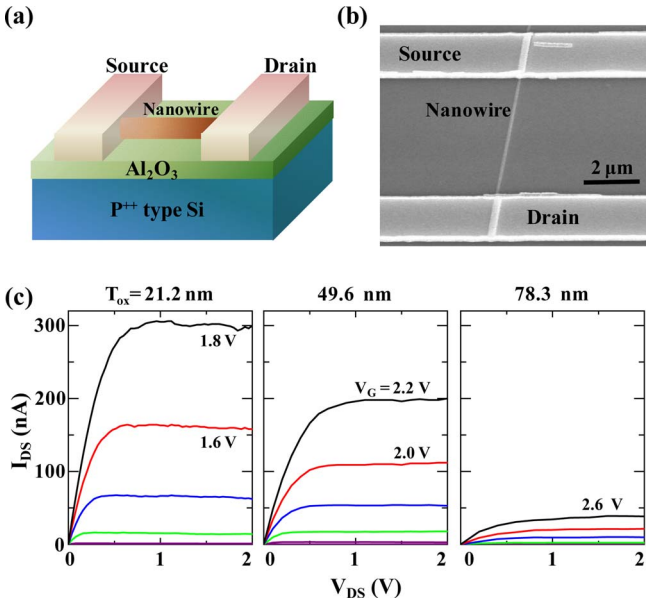

FIG. 2. (Color online) (a) Schematic of a ZnO nanowire FET device structure. (b) Scanning electron microscopy image of a single ZnO nanowire connected between source and drain electrodes in a FET device. (c) A series of $I_{DS}-V_{DS}$ characteristics for ZnO nanowire FETs with varying Al_2O_3 dielectric thicknesses (21.2, 49.6, and 78.3 nm).

III. RESULTS AND DISCUSSION

A. Analysis of high-*k* Al_2O_3 dielectrics

Figure 1(a) shows the cross-sectional HRTEM image of 21.2 nm thick Al_2O_3 dielectric layer and the insert shows schematic of a MOS device structure. An interfacial SiO_2 layer and an Al_2O_3 layer were clearly distinct in this figure. From C-V measurements with MOS structure, the equivalent oxide thickness (EOT) was calculated using an NCSU CVC program, which is an analysis program used to extract thin oxide parameters.[13] It is from the EOT as a function of the Al_2O_3 layer thickness that the dielectric constant and interfacial layer thickness are extracted. The plot in Fig. 1(b) represents the function

$$\mathrm{EOT} = \frac{k_{SiO_2}}{k_{Al_2O_3}} t_{Al_2O_3} + t_{SiO_2}, \quad (1)$$

where k_{SiO_2} and $k_{Al_2O_3}$ are the dielectric constants for Al_2O_3 and SiO_2, respectively, $t_{Al_2O_3}$ is the Al_2O_3 thickness, and t_{SiO_2} is the thickness of the SiO_2 interfacial layer. The slope of this plot yields an Al_2O_3 dielectric constant of ~7.55, and the *y*-intercept of the plot reveals the SiO_2 interfacial layer thickness to be ~1.46 nm. The dielectric constant of the Al_2O_3 layer has been reported in the range of 7–10, and it seems to depend on detailed growth conditions such as deposition process, growth temperature, precursor gas, and annealing treatment.[14–16] The interfacial SiO_2 layer thickness (~1.46 nm) extracted from the EOT versus the Al_2O_3 layer thickness [Fig. 1(b)] is consistent with the observed interfacial SiO_2 layer thickness (~1.54 nm) from HRTEM image.

The key advantage of using Al_2O_3 dielectrics is the reduction in leakage current compared to SiO_2 dielectrics with equal EOT values. Figure 3(a) displays the leakage current density versus applied voltage, measured from MOS struc-

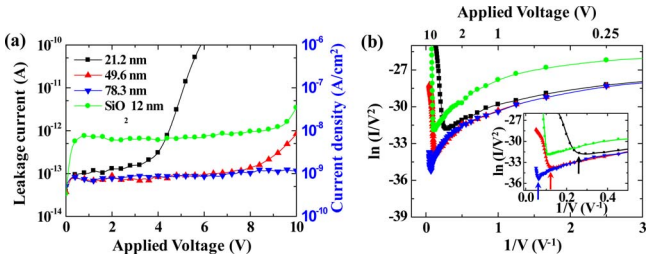

FIG. 3. (Color online) (a) Leakage current density vs applied voltage through Al_2O_3 dielectric layers of different thicknesses (21.2, 49.6, and 78.3 nm) and a 12 nm SiO_2 layer. (b) $\ln(I/V^2)$ vs 1/V plot for Al_2O_3 and 12 nm SiO_2 dielectric layers. Inset is a zoomed-in plot near the transition voltages (marked by arrows) from DT to FN tunneling (see text in detail).

ture devices with Al_2O_3 dielectric layers (thicknesses of 21.2, 49.6, and 78.3 nm) and SiO_2 layer (12 nm thick). The SiO_2 layer thickness of 12 nm was chosen for comparison because the EOT value of the 21.2 nm thick Al_2O_3 layer was determined as 12 nm from Eq. (1). This leakage current is the sum of the quantum-mechanical tunneling current through the dielectric layers and the charging current associated with the capacitance values of the dielectric layers. As shown in Fig. 3(a), the leakage current was shown to decrease with increasing thickness of the Al_2O_3 layer. The leakage current density for the Al_2O_3 layers was very low on the order of 1 nA/cm^2 when the applied bias was not too high, indicating the excellent insulating behavior of Al_2O_3 dielectric layers. Groner *et al.* also reported that the leakage current for Al_2O_3 layers of thickness between 3 and 115 nm was in the range of 10 to 0.1 nA/cm^2.[5] As shown in Fig. 3(a), the observed leakage current for the 12 nm SiO_2 layer ($\sim$10 nA/cm^2) was about ten times higher than that of the 21.2 nm Al_2O_3 layer ($\sim$1 nA/cm^2) when the applied bias was less than 4 V. At above 4 V, the leakage current for the 21.2 nm Al_2O_3 layer increased dramatically more than that for the 12 nm SiO_2 layer. This behavior can be explained by FN tunneling through the dielectric layer. When the applied bias is less than the barrier height of an insulating dielectric layer, DT occurs, whereas when the applied bias is higher than the barrier height, FN tunneling occurs.

In order to analyze the tunneling characteristics, we investigated the transition of DT to FN tunneling for all three Al_2O_3 layers (21.2, 49.6, and 78.3 nm thick) and the SiO_2 layer (12 nm thick), as shown in Fig. 3(b). Beebe *et al.*[17] reported that a plot of $\ln(I/V^2)$ versus 1/V exhibits logarithmic growth when the applied bias is less than the barrier height in the DT regime, whereas this plot exhibits a linear decay when the applied bias is higher than the barrier height in the FN tunneling regime. The transition from DT to FN tunneling accompanies a change in the barrier shape from trapezoidal to triangular, and it appears as an inflection in the plot of $\ln(I/V^2)$ versus 1/V.[17] Thus, the transition voltage provides a means of experimentally estimating the height of the original rectangular barrier. The inflection point (i.e., the barrier height) was observed to decrease as the thickness of the Al_2O_3 dielectric layer was decreased [Fig. 3(b)]. This behavior is clearly seen in the zoomed-in plot near the transition voltages [the inset of Fig. 3(b)]. Specifically, the transition voltage was observed as $\sim$3.4, 7.6, and 13.6 V for 21.2, 49.6, and 78.3 nm thick Al_2O_3 dielectric layers, respectively. For the 12 nm SiO_2 case, the transition voltage was observed to be $\sim$8.6 V. FN tunneling at relatively small bias ($\sim$3.4 V) for the 21.2 nm thick Al_2O_3 dielectric layer explains the dramatic increase in leakage current above $\sim$3.4 V, as well as the fact that its leakage current is higher than that of the 12 nm SiO_2 layer above $\sim$4 V [Fig. 3(a)]. Note that Ng *et al.*,[18] reported a similar trend of barrier height dependence on the thickness of SiO_xN gate dielectric layer.

B. Electrical properties of ZnO nanowire transistors

The ZnO nanowire FETs with high-k Al_2O_3 dielectric layers (thicknesses of 21.2, 49.6, and 78.3 nm) were fabricated to investigate their electrical properties. The FET device schematic and FESEM image of a fabricated device are shown in Figs. 2(a) and 2(b), respectively. During the electrical measurements, the current-voltage characteristics of the ZnO nanowire FETs were restricted in a voltage range less than 3 V, since FN tunneling current in MOS devices with 21.2, 49.6, and 78.3 nm thick Al_2O_3 and 12 nm SiO_2 dielectric layers is negligible below 3 V [Fig. 3(b)]. Figure 2(c) shows a series of source-drain current versus drain voltage (I_{DS}-V_{DS}) characteristics of the ZnO nanowire FETs with Al_2O_3 dielectric layers. In all cases, the I_{DS}-V_{DS} curves exhibited well-defined linear regimes at low bias levels and saturation regimes at high bias levels. This is typical electrical behavior for n-type FETs. The gate bias for on-current state is dependent on the dielectric layer thickness. As the dielectric layer thickness decreased, the current increased. This trend is due to the increased carrier modulation efficiency by the gate bias through the thinner dielectric layer. In other words, a higher gate bias is needed in nanowire FETs with a thicker dielectric layer to maintain the on-current state.

Figure 4(a) displays the source-drain current versus the gate voltage (I_{DS}-V_G) characteristics of ZnO nanowire FETs with Al_2O_3 dielectric layers, measured at a fixed drain bias of 80 mV. The dispersion of the threshold voltage (V_T) values was obtained by taking statistical averages and standard deviations of sets of individual nanowire FETs (three to five FET devices at each data point), as summarized in the inset of Fig. 4(a). The V_T value decreased as the dielectric layer thickness decreased, indicating a successful gate modulation. Specifically, we observed V_T values of 1.2 ± 0.1, 1.7 ± 0.1,

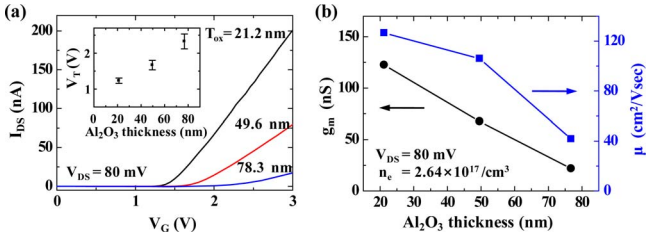

FIG. 4. (Color online) (a) $I_{DS}-V_G$ characteristics for ZnO nanowire FETs with varying Al_2O_3 dielectric thicknesses at fixed V_{DS}=80 mV. The inset shows the statistical distribution of the measured threshold voltage. (b) Transconductance (g_m) and mobility (μ) of ZnO nanowire FETs with varying Al_2O_3 dielectric thicknesses.

and 2.3 ± 0.2 V for ZnO nanowire FETs with dielectric layer thicknesses of 21.2, 49.6, and 78.3 nm, respectively. The V_T values are influenced by several factors, such as the dielectric material, various charges and traps in the dielectric, the substrate doping conditions, and the device dimensions.[19] In our study, the increase in dielectric thickness resulted in a V_T shift to the positive gate bias direction. This means that a higher gate bias is needed to turn on the nanowire FET with a thicker dielectric layer.

Figure 4(b) shows the transconductance ($g_m = dI_{DS}/dV_G$) and mobility (μ) for ZnO nanowire FETs with Al_2O_3 dielectric layers. Mobility of ZnO nanowire FETs can be calculated from the equation

$$\mu = \frac{g_m L^2}{V_{DS} C_G}, \tag{2}$$

where L is the nanowire channel length (~ 4 μm), and C_G is the gate capacitance. Here, C_G can be estimated from the model of a cylinder on an infinite metal plate,[20] $C_G = 2\pi\varepsilon_0\varepsilon_r L/\cosh^{-1}(1+T_{OX}/r)$; herein, r is the nanowire radius (~ 50 nm), T_{OX} is the dielectric thickness (21.2, 49.6, and 78.3 nm), ε_0 is the permittivity of free space, and ε_r ($=k_{Al_2O_3}$) is the dielectric constant of Al_2O_3 [7.55 determined from Fig. 1(b)]. We calculated the mobility at the equal carrier concentration ($\sim 2.64 \times 10^{17}$ cm^{-3}) in ZnO nanowire FETs with different dielectric layer thicknesses, since the scattering is susceptible to carrier concentration and surface roughness. With this reason, the transconductance for calculating mobility was extracted from the gate voltage at an equal carrier concentration ($\sim 2.64 \times 10^{17}$ cm^{-3}) that was chosen arbitrary and was calculated as ~ 123 ns (at $V_G = 1.9$ V), ~ 67.5 ns ($V_G = 2.7$ V), and ~ 21.8 ns ($V_G = 3.6$ V) for the ZnO nanowire FETs with dielectric thicknesses of 21.2, 49.6, and 78.3 nm, respectively, as shown in Fig. 4(b) (left axis). As the dielectric thickness decreased, both transconductance and capacitance increased. However, the transconductance increased dominantly, resulting in the increase of the mobility which was found to be ~ 127, ~ 106, and ~ 41.7 cm^2/V s for 21.2, 49.6, and 78.3 nm dielectric layer thicknesses, respectively, as shown in Fig. 4(b) (right axis). Note that Bhowmick *et al.*[21] theoretically predicted an increase in transconductance as decreasing the gate oxide thickness for silicon nanowire FETs.

IV. CONCLUSIONS

In conclusion, we investigated the electrical characteristics of ZnO nanowire FETs with high-k Al_2O_3 dielectrics of different thickness. For MOS structure with Al_2O_3 dielectrics, the leakage current was reduced as compared with conventional SiO_2 gate oxides, which was characterized by the transition of DT to FN tunneling. For ZnO nanowire FETs, as the thickness of the Al_2O_3 dielectric layer was reduced, the electrical conductance, transconductance, and mobility increased, and the threshold voltage shifted to the negative bias direction.

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