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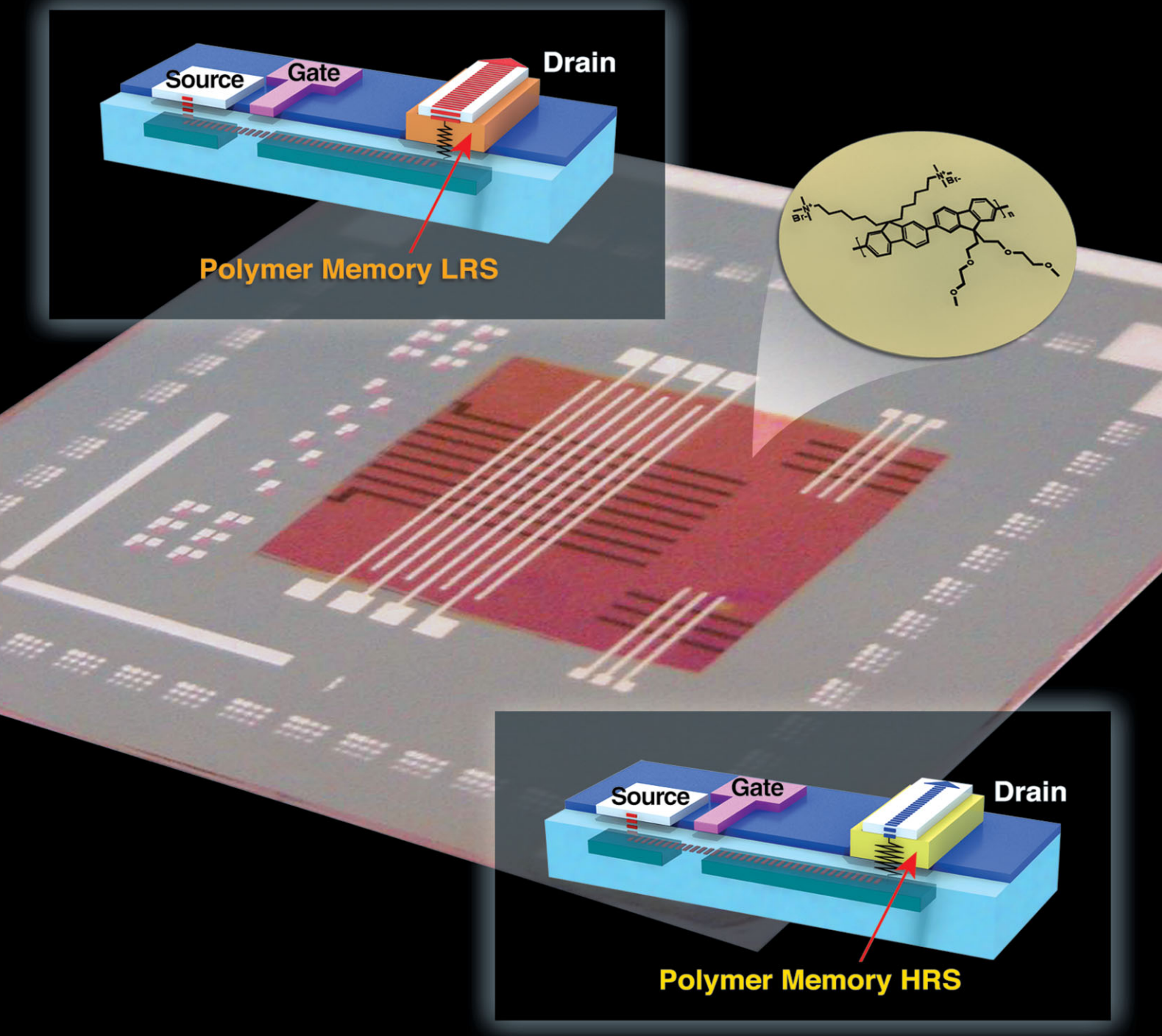

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Single Transistor/Resistor Memory

ADVANCED MATERIALS

One Transistor–One Resistor Devices for Polymer Non-Volatile Memory Applications

By *Tae-Wook Kim, Hyejung Choi, Seung-Hwan Oh, Gunuk Wang, Dong-Yu Kim, Hyunsang Hwang,* and *Takhee Lee**

Over the past decade, organic electronics have been investigated due to their various merits, such as low cost, flexibility, easy fabrication, and printing capability.[1–5] Many researchers have reported high-performance organic light-emitting diodes (OLEDs), organic thin-film transistors (OTFTs), and organic photovoltaics (OPVs).[1–5] In addition, with the rapid development of information technology, organic memory has become an important field for data-storage applications. Since Silva et al. reported the first organically based bistable memory devices,[6] many research groups have tried to develop novel polymer materials, optimal device structures, and fabrication methods for practical organic memory applications.[7–17] Recently, single-layer polymer non-volatile memory devices with a vertical metal–insulator–metal (MIM) structure were demonstrated.[16–18] A direct metal–transfer method was introduced to fabricate cross-point-type organic memory devices with a $2\,\mu m \times 2\,\mu m$ cell size.[19] In addition, multilevel cells and multilayer stacking structures have been proposed to achieve high data-storage densities.[20–23]

In spite of the extensive fundamental research on polymer memory devices, there have been little publications related to integrated polymer memory devices consisting of switch (transistor or diode) and memory (resistor) components. When polymer nonvolatile memory devices are scaled down and fabricated in a cross-point-type array structure, switch components, such as transistors or diodes, are indispensable to prevent unexpected crosstalk. These effects are caused by the misreading of the resistance state via low-resistance paths through unselected neighboring polymer memory cells, or an excess of current that may induce electrical damages in the memory element.[24–26] Therefore, fabrication and characterization of both transistors and polymer memory in one chip are essential. The single-transistor and memory (one transistor and one resistor; 1T–1R), or single-diode and memory (one diode and one resistor; 1D–1R) structure is a promising building block for achieving random accessibility in polymer nonvolatile memory applications. Particularly, 1T–1R or 1D–1R structures were suggested as a cell element for macromolecular memories (polymer memory) by the International Technology Roadmap for Semiconductors (ITRS).[27]

[*] Prof. T. Lee, T.-W. Kim, H. Choi, S.-H. Oh, G. Wang, Prof. D.-Y. Kim, Prof. H. Hwang
Heeger Center for Advanced Materials
Department of Materials Science and Engineering
Gwangju Institute of Science and Technology
1 Oryong-Dong, Buk-Gu
Gwangju 500-712 (Korea)
E-mail: tlee@gist.ac.kr

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In the field of inorganically based memory, combinations of switch and memory components have been extensively investigated. 1T–1R- and 1D–1R-type circuits have been demonstrated in devices such as resistive-change random-access memory (ReRAM) and phase-change random-access memory (PRAM).[24–26,28] On the other hand, the poor processability of organic materials compared to inorganic materials has been one of the major obstacles to achieving more integrated circuitry for practically all organically based electronics applications. For this reason, the feasibility of producing an organically based 1T–1R circuit that consists of a transistor and a polymer memory should be explored.

In this paper, we demonstrate that 1T–1R hybrid-type devices consisting of a silicon transistor (p-MOSFET) and a resistive polymer memory can be used as a nonvolatile memory-cell element. Our results show that the operation of 1T–1R devices can be controlled by the resistance states of the polymer memory device. Our 1T–1R devices were successfully operated by applying consecutive voltage pulses to the polymer memory. Written or erased data in the 1T–1R devices was maintained for more than 10^4 s, indicating promise as potential 1T–1R polymer memory devices.

Figure 1 shows schematics and images of 1T–1R devices. The operation of a one-bit cell device (1T–1R device) is controlled by

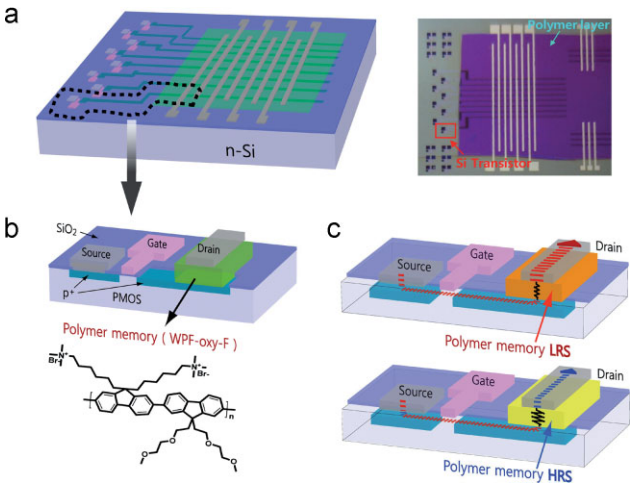

Figure 1. a) Schematic and optical image of 1T–1R hybrid devices. The area with the black dotted line indicates a silicon transistor (1T) and a polymer memory (1R). b) Schematic of a single 1T–1R device and chemical structure of WPF-oxy-F. c) Schematics of basic operation of the 1T–1R device. The current flow from source to drain in the 1T–1R device is controlled by the resistance state of the polymer memory device (see text).

two electronic parts consisting of a p-channel metal oxide semiconductor field-effect transistor (MOSFET) and a polymer memory device. Figure 1a shows the schematic and optical image of 1T–1R devices fabricated on a silicon substrate. Figure 1b shows the schematic of the one-bit cell 1T–1R device and the chemical structure of the organic memory material used in our study, the polyfluorene-derivative poly[(9,9-bis((6′-(*N*,*N*,*N*-trimethylammonium)hexyl)-2,7-fluorene)-*alt*-(9,9-bis(2-(2-methoxyethoxy) ethyl)-fluorene)] Dibromide (denoted WPF-oxy-F). The p-MOSFET device was fabricated in a conventional complementary metal oxide semiconductor (CMOS) process. In this work, all fabrication was performed under 150 °C. One should consider the thermal robustness of polymer material for commercialized fabrication process and reliable operation of 1T–1R device.

A polymer nonvolatile memory device with crosspoint architecture was fabricated on the drain side (p^+ Si) of the Si transistor, which was used as the bottom electrode (Fig. 1b). Note that we used a p-MOSFET device as a switch component instead of fabricating all organically based 1T–1R devices. When organic-transistor and organic-resistor layers are formed by spin-coating or thermal evaporation, they may dissolve each other. It is generally difficult to fabricate both organic transistors and organic resistors in one chip without damaging the active layers and with no degradation of the device. Furthermore, the operating voltage of the organic thin-film transistors (OTFTs) is typically much higher than that of polymer memory devices.[29] For these reasons, we adopted the hybrid approach, combining inorganic transistors and organic resistors.

Figure 1c shows schematics illustrating the basic operation of the 1T–1R device. When the switch component (p-MOSFET) is turned ON, the current from source to drain is modulated by the polymer memory (1R), which has two stable resistance states: a high-resistance state (HRS) and a low-resistance state (LRS). We first performed current–voltage (*I*–*V*) characterization on the p-MOSFET devices and polymer memory devices individually. Figure 2a presents the drain current versus drain voltage (I_D–V_D) characteristic of the p-MOSFET device and its circuit diagram (inset). The gate width and length are both 20 μm. In order to switch the p-MOSFET device ON, we applied a negative bias to the gate electrode. The drain current was saturated at about −70 μA for a gate bias of −2.0 V, exhibiting typical long-channel p-MOSFET behavior. We also performed *I*–*V* characterization on the polymer memory device. Figure 2b shows a clear bipolar switching with bistable resistance states of HRS and LRS. Unlike unipolar switching devices, in the bipolar devices, resistive switching occurred for different bias polarities. The polymer memory device displayed in Figure 2b exhibited turn-ON and turn-OFF events occurring at ≈3 V and −2 V, respectively. In our previous works, we reported WPF-oxy-F polymer (Fig. 1b) as a potential active material for polymer memory devices.[18,19,30] In the metal–insulator–metal or crosspoint architecture, WPF-oxy-F polymer showed a typical bipolar switching behavior with an ON/OFF ratio of more than three orders of magnitude.[18,19,30]

To evaluate *I*–*V* characteristics of the p-MOSFET connected to the polymer memory, we also measured the I_D–V_D and drain current versus gate voltage (I_D–V_G) characteristics of the 1T–1R device. As shown in Figure 3a, when the polymer memory device is in the LRS condition, the 1T–1R device had I_D–V_D curve very similar to that of the p-MOSFET device alone, indicating that the polymer memory in the LRS condition does not affect the operation of the transistor. However, because of the series resistance of both the channel and the polymer memory, the current level in the 1T–1R device (Fig. 3a) in the saturation regime was reduced by a factor of ≈0.7 compared to the single transistor (Fig. 2a) under the same gate bias. In contrast, when the polymer memory device is turned to the HRS, the current flow from source to drain in the p-MOSFET device was significantly

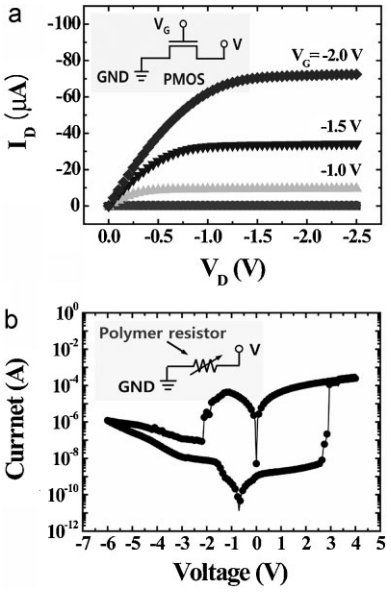

Figure 2. a) I_D–V_D characteristics of the p-MOSFET device and its circuit diagram. b) *I*–*V* characteristics of polymer memory device and its circuit diagram.

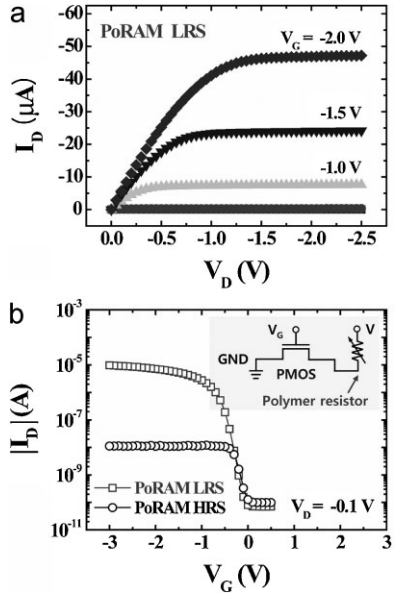

Figure 3. a) I_D–V_D characteristics of the 1T–1R device. b) I_D–V_G characteristics of the 1T–1R device with respect to the resistance state of polymer memory device.

interrupted by the high resistance of the polymer memory device. In the HRS condition, only ≈10 nA current flowed from source to drain through the 1T–1R device under a gate bias of −2 V. Similar behavior was also observed in the I_D–V_G curve of the 1T–1R device at a fixed drain bias of −0.1 V, as shown in Figure 3b. The drain current for the 1T–1R device in the saturation regime was observed as 10 μA (in LRS condition) and 10 nA (in HRS condition). The difference in drain current was about three orders of magnitude, indicating that the drain current of the 1T–1R device can be controlled by the resistance states of the polymer memory device at a fixed drain bias.

The performance of the 1T–1R memory devices was also investigated. The endurance of the 1T–1R device subjected to consecutive single voltage pulses applied to the polymer memory device is shown in Figure 4a. The LRS and HRS of the polymer memory in the 1T–1R device were alternated via a 5 V pulse (writing process, V_P) and a −4 V pulse (erasing process, V_E), with a pulse duration (τ_p) of 30 and 200 ms, respectively. The current value of the 1T–1R device was then read at a fixed gate bias of −1.0 V and drain bias of −0.1 V. During 50 repetitions of voltage pulses, our 1T–1R device operated successfully, exhibiting an I_{ON}/I_{OFF} ratio of more than $\approx 10^3$. Note that switching events under faster voltage pulses are required for practical memory applications. The retention characteristic was also investigated under ambient conditions at room temperature, as shown in Figure 4b. We measured the I_D–V_G of the 1T/1R device at a fixed gate bias of −1.0 V and drain bias of −0.1 V when the polymer memory was set as either HRS or LRS. The two current values of the 1T–1R device, corresponding to the HRS and LRS of the polymer memory device, were maintained for 10^4 s without any significant degradation. In addition, we did not observe any damages in the dielectric layer during operation of the transistor (1T).

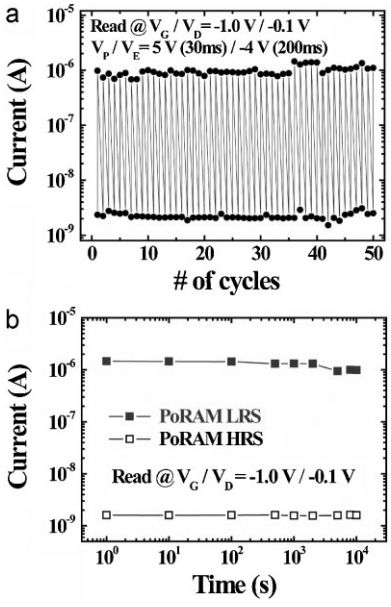

Figure 4. a) The endurance of the 1T–1R device with consecutive single voltage pulses applied to the polymer memory device. The measurement conditions are a 5 V pulse (writing process, V_P) and a −4 V pulse (erasing process, V_E) with pulse duration (τ_p) of 30 and 200 ms, respectively. b) Retention characteristics of the 1T–1R device. The current value was read at a fixed gate of −1.0 V and drain bias of −0.1 V.

In conclusion, we successfully demonstrated 1T–1R hybrid memory devices consisting of a silicon transistor (p-MOSFET) and a polymer memory. Individual p-MOSFET and polymer memory devices exhibited typical p-channel transistor and nonvolatile memory properties, respectively. The 1T–1R memory device was successfully switched by applying consecutive voltage pulses to the polymer memory. The written or erased data in the 1T–1R device was maintained for more than 10^4 s.

Experimental

The novel structure p-MOSFET was fabricated on an n-type (100) silicon substrate (resistivity of 4–6 Ω · cm). After the isolation was defined, 50 Å thick SiO_2 was grown by dry oxidation to form the gate oxide. Subsequently, 2000 Å thick undoped polysilicon was deposited on the gate oxide layer. Gate electrodes were made by photolithography and wet etching of the polysilicon. Boron implantation was then performed at 20 keV, followed by a rapid thermal-annealing (RTA) process. The Si doped Al (1% of Si) electrode layer was deposited on the source electrodes, while the drain electrodes were left open for connection to the polymer memory layer. After defining the source and drain electrodes, forming-gas annealing was performed at 400 °C for 30 min under nitrogen and hydrogen mixture gas (N_2 97% + H_2 3%) atmosphere. The resulting transistor-device structure has a gate width and gate length of 20 μm.

As a polymer resistor layer, WPF-oxy-F was synthesized using a palladium-catalyzed Suzuki coupling reaction method [31]. WPF-oxy-F was first dissolved in methanol at a concentration of 10 mg mL^{-1} and was then spin-coated on the substrate. The typical spin-coating condition was 2000 rpm for 30 s. Post-baking was performed at 150 °C for 20 min on a hotplate in a nitrogen-filled glove box. To form electrodes on top of the polymer layer, a shadow mask with a line width of 100 μm was aligned and a 100 nm thick Ag layer was deposited using a thermal evaporator under a pressure of 10^{-6} Torr (1 Torr = 133.32 Pa). The device area of the polymer memory is 100 μm × 100 μm, which is defined by the crosspoint area of the junction and top electrode. The current–voltage (*I*–*V*) measurements were carried out using a semiconductor parameter analyzer (Agilent Technology 4155C) with pulse generator units (Agilent 41501B PGUs)

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[1] C. D. Müller, A. Falcou, N. Reckefuss, M. Rojahn, V. Wiederhirn, P. Rudati, H. Frohne, O. Nuyken, H. Becker, K. Meerholz, *Nature* **2003**, *421*, 829.
[2] G. Darlinski, U. Böttger, R. Waser, H. Klauk, M. Halik, U. Zschieschang, G. Schmid, C. Dehm, *J. Appl. Phys.* **2005**, *97*, 093708.
[3] T. W. Lee, Y. Byun, B. W. Koo, I. N. Kang, Y. Y. Lyu, C. H. Lee, L. Pu, S. Y. Lee, *Adv. Mater.* **2005**, *17*, 2180.
[4] J. Y. Kim, K. Lee, N. E. Coates, D. Moses, T. Q. Nguyen, M. Dante, A. J. Heeger, *Science* **2007**, *317*, 222.
[5] S.-I. Na, S.-S. Kim, J. Jo, D.-Y. Kim, *Adv. Mater.* **2008**, *20*, 4061.

[6] P. O. Slvia, G. Dir, C. Griffiths, *J. Non-Cryst. Solids* **1970**, *2*, 316.
[7] S. Barman, F. Deng, R. L. McCreery, *J. Am. Chem. Soc.* **2008**, *130*, 11073.
[8] L. D. Bozano, B. W. Kean, M. Beinhoff, K. R. Carter, P. M. Rice, J. C. Scott, *Adv. Funct. Mater.* **2005**, *15*, 1933.
[9] M. Karakawa, M. Chikamatsu, Y. Yoshida, R. Azumi, K. Yase, C. Nakamoto, *Macromol. Rapid Commun.* **2007**, *28*, 1479.
[10] C. H. Tu, Y. S. Lai, D. L. Kwong, *IEEE Electron Device Lett.* **2006**, *27*, 354.
[11] A. Bandhopadhyay, A. J. Pal, *J. Phys. Chem. B* **2003**, *107*, 2531.
[12] B. Mukherjee, A. J. Pal, *Appl. Phys. Lett.* **2004**, *85*, 2116.
[13] J. Ouyang, C. W. Chu, C. R. Szmanda, L. Ma, Y. Yang, *Nat. Mater.* **2004**, *3*, 918.
[14] R. J. Tseng, C. Tsai, L. Ma, J. Ouyang, C. S. Ozkan, Y. Yang, *Nat. Nanotechnol.* **2006**, *1*, 72.
[15] Y. Chen, G. Y. Jung, D. A. A. Ohlberg, X. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart, R. S. Williams, *Nanotechnology* **2003**, *14*, 462.
[16] C. Pearson, J. H. Ahn, M. F. Mabrook, D. A. Zeze, M. C. Petty, K. T. Kamtekar, C. Wang, M. R. Bryce, P. Dimitrakis, D. Tsoukalas, *Appl. Phys. Lett.* **2007**, *91*, 123506.
[17] Q.-D. Ling, E.-T. Kang, K.-G. Neoh, Y. Chen, X.-D. Zhuang, C. Zhu, D. S. H. Chan, *Appl. Phys. Lett.* **2008**, *92*, 143302.
[18] T.-W. Kim, S.-H. Oh, H. Choi, G. Wang, D.-Y. Kim, H. Hwang, T. Lee, *Appl. Phys. Lett.* **2008**, *92*, 253308.
[19] T.-W. Kim, K. Lee, S.-H. Oh, G. Wang, D.-Y. Kim, G.-Y. Jung, T. Lee, *Nanotechnology* **2008**, *19*, 405201.
[20] M. Caironi, D. Natali, E. Canesi, A. Bianco, C. Bertarelli, G. Zerbi, M. Sampietro, *Thin Solid Films* **2008**, *516*, 7680.
[21] B.-O. Cho, T. Yasue, H. Yoon, M.-S. Lee, I.-S. Yeo, U.-I. Chung, J.-T. Moon, B.-I. Ryu, *IEEE Int. Electron. Devices Meet. Tech. Dig.* **2006**, DOI: 10.1109/IEDM.2006.346729.
[22] W. L. Kwan, R. J. Tseng, W. Wu, Q. Pei, Y. Yang, *IEEE Int. Electron. Devices Meet. Tech. Dig.* **2007**, 237.
[23] H.-T. Lin, Z. Pei, J.-R. Chen, C.-P. Kung, Y.-C. Lin, C.-M. Tseng, Y.-J. Chan, *IEEE Int. Electron. Devices Meet. Tech. Dig.* **2007**, 233.
[24] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, Y. Sugiyama, *Appl. Phys. Lett.* **2008**, *93*, 033506.
[25] M.-J. Lee, Y. Park, D.-S. Suh, E.-H. Lee, S. Seo, D.-C. Kim, R. Jung, B.-S. Kang, S.-E. Ahn, C. B. Lee, D. H. Seo, Y.-K. Cha, I.-K. Yoo, J.-S. Kim, B. H. Park, *Adv. Mater.* **2007**, *19*, 3919.
[26] B. S. Kang, S.-E. Ahn, M.-J. Lee, G. Stefanovich, K. H. Kim, W. X. Xianyu, C. B. Lee, Y. Park, I. G. Baek, B. H. Park, *Adv. Mater.* **2008**, *20*, 3066.
[27] International Technology Roadmap for Semiconductors, ITRS, **2007**, http://www.itrs.net/.
[28] M.-J. Lee, S. Seo, D.-C. Kim, S.-E. Ahn, D. H. Seo, I.-K. Yoo, I.-G. Baek, D.-S. Kim, I.-S. Byun, S.-H. Kim, I.-R. Hwang, J.-S. Kim, S.-H. Jeon, B. H. Park, *Adv. Mater.* **2007**, *19*, 73.
[29] Y.-Y. Lin, D. J. Gundlach, S. F. Nelson, T. N. Jackson, *IEEE Trans. Electron Devices* **1997**, *44*, 1325.
[30] T.-W. Kim, S.-H. Oh, H. Choi, G. Wang, H. Hwang, D.-Y. Kim, T. Lee, *IEEE Electron Device Lett.* **2008**, *29*, 852.
[31] S.-H. Oh, S.-I. Na, Y.-C. Nah, D. Vak, S.-S. Kim, D.-Y. Kim, *Org. Electron.* **2007**, *8*, 773.