Nanoscale Resistive Switching of a Copper–Carbon-Mixed Layer for Nonvolatile Memory Applications

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***Abstract*—The nanoscale resistance switching property of copper–carbon-mixed (Cu–C) layer was investigated for nonvolatile memory applications. The Cu–C layer of the cross-point cell array showed typical filament switching with two orders of on/off ratio, exhibiting stable resistance switching and a narrow distribution of set and reset voltages in the nanoscale junction. In addition, we investigated the area dependence of operation current. Based on these results and current–voltage dependence on temperature, we discussed a potential switching mechanism of Cu–C layer.**

***Index Terms*—Cell array, copper–carbon-mixed (Cu–C) layer, resistance random access memory, resistive switching.**

I. Introduction

RESISTANCE random access memory shows great promise for use in next-generation nonvolatile memory due to its excellent scalability, low power consumption, and nondestructive readout [1], [2]. Recently, solid-state electrolyte memory based on silver and copper ions has become more attractive. In particular, chalcogenide materials, such as CuS and AgS, have been reported as possible resistive switching materials [3], [4]. The switching mechanism is the result of conductive materials, such as Cu ions, which are incorporated into the solid-state electrolyte, creating a conducting filament. During operation, the conducting filament can receive and release Cu ions when a programming voltage is applied. However, too low switching voltage, nonuniformity, and poor retention characteristics need to be improved before they can be used in practical memory applications. The requirement of a low operation current, which is related to speed, power consumption, and heat generation [5], needs to be addressed. In addition, the specific mechanism at microscale regions is still uncertain [5].

Although there have been several efforts aimed at improving these properties by replacing chalcogenides with insulating oxide, doing so has required more than ternary elements and complicated process [6]–[10]. In this letter, we used carbon instead of chalcogenides because it is a good alternative solid-state electrolyte based on various qualities, including its property as an insulator and its high Cu diffusivity [11]–[13]. In this letter, we investigated the nanoscale memory characteristics of new carbon-based resistive switching materials.

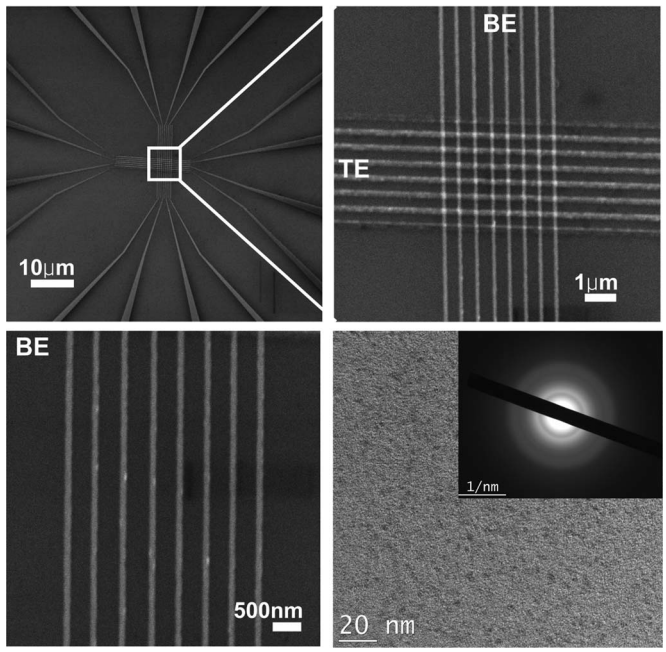

Fig. 1. SEM images of the cell array with 100-nm-width line and 500-nm pitch, as well as the plan-view TEM image of the Cu–C layer.

II. Experimental Setup

An 8×8 cell array was fabricated on a 3000-Å-thick thermal oxide grown on a Si substrate. The bottom and top electrodes (BE and TE, respectively) were patterned by e-beam lithography and the liftoff method. Platinum metal was deposited by an e-beam evaporator. The width of the cell array was 100 or 300 nm with a space of 400 nm. After formation of the BE, a copper–carbon-mixed (Cu–C) layer was deposited by RF magnetron sputtering at room temperature using a Cu target in an atmosphere comprised of a mixture of CH_4, O_2 and Ar gases, where O_2 gas was used as a catalyst for the decomposition of CH_4 gas [14]. The composition ratio of Cu to C was 1.5, as determined by X-ray photoemission spectroscopy [13]. The

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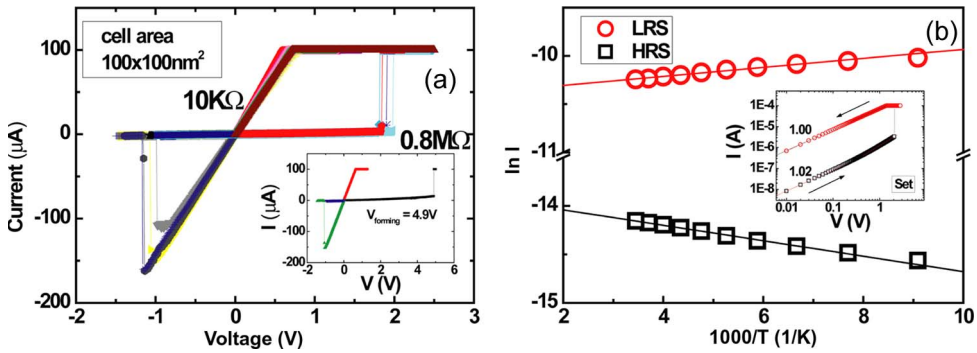

Fig. 2. (a) Typical I–V hysteresis of one cell in the cell array. The inset shows the forming process. (b) Temperature-variable I–V measurements in the temperature range from 100 K to 300 K. The inset shows I–V characteristics in a double-logarithmic plot at the positive bias region.

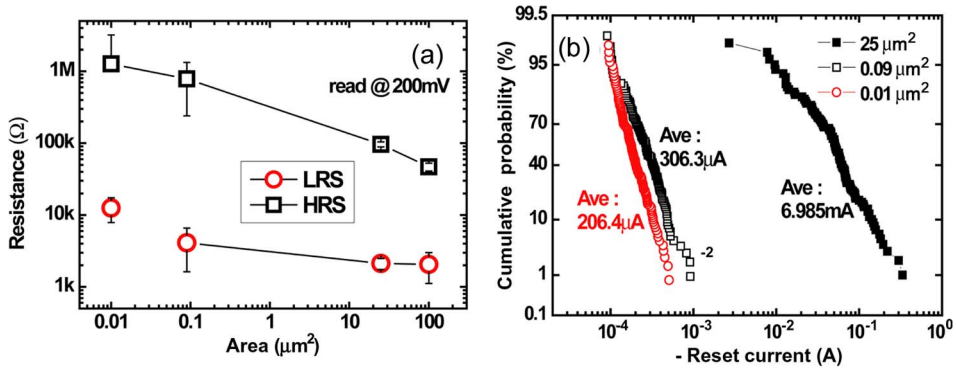

Fig. 3. (a) Cell area dependence of HRS and LRS. (b) Distribution of reset current for different cell arrays. The average value is indicated.

thickness of the Cu–C layer was 70 nm, as measured by cross-sectional scanning electron microscopy (SEM). Subsequently, the TE was patterned on the Cu–C surface. The memory cell was defined by the cross point of the BE and the TE without etching of the Cu–C layer. The SEM images of the fabricated cell array and a plan-view transmission electron microscopy (TEM) image of the Cu–C layer are shown in Fig. 1. Using an HP4155C semiconductor parameter analyzer and a probe station, I–V measurements demonstrated the device to be operating as a memory device.

III. Results and Discussion

Fig. 2(a) shows the typical current–voltage (I–V) hysteresis of a 100 × 100-nm^2 cell in the cell array. For resistive switching, the Cu–C material required a forming process around 5 V, as shown in the inset of Fig. 2(a). As we applied a positive bias from 0 to 2.5 V to the Pt TE, the current increased abruptly at around 2 V, indicating set operation. To prevent electrical breakdown of the device, the current compliance was set at 100 μA. Then, the bias voltage was applied in the reverse direction, from 2.5 to -1.5 V. A sharp decrease in the current was observed near -1 V, which is the reset. This device shows a bistable resistance state with a high resistance ratio of 10^2.

The switching mechanism of Cu–C was investigated. The plan-view TEM image of the carbon-incorporated copper showed amorphous phase without Cu grain, as shown in Fig. 1. It means that carbon atoms contribute to the reduction of Cu grain size and increase of electrical resistivity [11]. To understand the switching mechanism [15], the log–log plot of this I–V hysteresis at the set region is shown in the inset of Fig. 2(b), which shows ohmic behavior with a slope of one in both states. In addition, the charge transport mechanism was studied in the temperature range from 100 K to 300 K. Fig. 2(b) shows the Arrhenius plot of the high-resistance state (HRS) and low-resistance state (LRS) currents. The currents were read at 0.2 V, while the temperature was swept at a speed of 2 K/min. The HRS current can be explained as a thermally activated transport. On the other hand, the LRS current is inversely proportional to the temperature, indicating metallic behavior [16]. Based on these results, Cu ions move and make the conducting path during the forming process. When negative bias was applied at TE, the Cu ions near the TE was released and broke the filaments.

The dependence of cell array resistance on area is shown in Fig. 3(a). For comparison, devices with areas of 10 × 10 and 5 × 5 μm^2, which were fabricated by photolithography, were also examined. HRS shows a weak dependence on cell area. The resistance of LRS shows a slight dependence on device size, indicating that the conducting path is localized. In the case of LRS of 0.01-μm^2-area cells, the thin and narrow metal line induced the increase of metal resistance and, hence, resistance of LRS. Based on these results, resistive switching of Cu–C materials can be explained by filament switching from formation and rupture of Cu filaments.

Low operation current is an important factor for low power consumption and heat generation [5]. Low set and reset currents are also important. The device of 0.01-μm^2 cells show resistive switching, even at 10 μA, and a resistance ratio of 10^2 (not shown here). Fig. 3(b) shows the distribution of reset currents

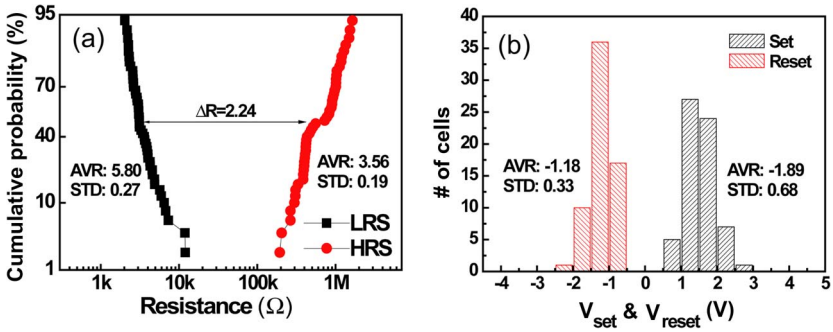

Fig. 4. (a) Cell-to-cell uniformity of resistance. (b) Fluctuations of $V_{\rm set}$ and $V_{\rm reset}$ from cell to cell.

for different cell areas during one cell endurance. The dc-voltage sweep range was from 3 to -3 V, and the compliance current was fixed at 100 μA. During the endurance test, the standard derivation of the distribution of resistance was kept at log (resistance) < 0.1. Here, the reset current is defined as the maximum current that can be attained before an abrupt decrease of current occurs at reset operation. This value shows the dependence on area of the reset current. Because LRS shows no dependence on area, it is expected that power consumption is reduced as the cell area is decreased. In addition, since our device consisted of Pt TE and BE, the source of the filament is not the metal electrode but the Cu ions in the Cu–C layers. Therefore, it can be concluded that the reset process is concerned not only with the electric field but also with joule heating. These low operation currents can provide the advantages which lend themselves to scalability and low-power devices.

For the analysis of device uniformity, we measured all cells in the 8×8 cell array. While measuring a specific memory cell in the array, the other cells were HRS and floating condition. Fig. 4(a) shows the cumulative probability of bistable resistance in all cells. The average and standard deviation of resistances are indicated in the figure. All data selected were obtained from the second hysteresis sweep. Comparing these results with the single-cell endurance results, the deviation of resistance from cell to cell was slightly greater. The distribution of $V_{\rm set}$ and $V_{\rm reset}$ of the 0.09-μm^2 cell array is shown in Fig. 4(b). Based on these results, even though the randomly formed filaments in the small cell array induced a voltage distribution, we also observed a narrow distribution of resistance states and cell-to-cell uniformity. However, further studies on random addressability and disturbance using one-diode/one-resistor or one-transistor/one-resistor structure are still necessary.

IV. Conclusion

The nanoscale resistance switching property of Cu–C was investigated in 8×8 cell array with 100-nm width. Typical filament switching was observed at I–V hysteresis, where operation voltage is higher than ± 1 V. Lower set and reset currents were observed when the cell area was decreased. In addition, fluctuations in resistance, set voltage $(V_{\rm set})$, and reset voltage $(V_{\rm reset})$ at 8×8 cells were analyzed. Nanoscale-sized Cu–C cell arrays showed stable resistance switching and a narrow distribution of set and reset voltages. The Cu–C layer can be one of the potential candidates for next-generation nonvolatile memory applications.

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