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Data retention characteristics of MANOS-type flash memory device with different metal gates at various levels of charge injection

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ABSTRACT

We investigated the impact of charge injection and metal gates (Al and Pt) on the data retention characteristics of metal–alumina–nitride–oxide–silicon (MANOS) devices for NAND flash memory application. Through the theoretical and experimental results, the highly injected charge (ΔV_{TH}) could cause the band bending of Al_2O_3, which reduced the tunneling distance across Al_2O_3. Thus, the dominant charge loss path is not only toward SiO_2 but also toward Al_2O_3 direction. Compared to low-metal work function (Φ_M), ONA stack with high-Φ_M showed better data retention characteristics, even if ΔV_{TH} is high. This could be explained by Fermi level alignment for different Φ_M, which results in the reduction of electric field across the Al_2O_3 compensated by the $\Delta\Phi_M$ ($\Phi_{Pt} - \Phi_{Al}$).

1. Introduction

The charge trap flash (CTF) memory based on the Si_3N_4 trapping layer has been continuously developed for the implement of massive storages [1,2]. To establish the excellent program/erase (P/E) speed and retention characteristics, the variety of approaches for the modulation of device structure has been explored. First, high-*k* top oxide (TPO) with high-metal work function (Φ_M) and band-gap engineered (BE) bottom oxide (BTO) were utilized to enhance the P/E speed [3,4]. The adoption of high-*k* dielectric as a TPO has an advantage to increase the electric field across the BTO at same physical thickness [5]. Recently, it was found that CTF memory with BE-BTO exhibited better erase speed when compared to a single SiO_2 BTO due to higher hole current by shortening of tunneling distance [6]. Secondly, with regard to the charge loss, the charge trapping layer with deep trap energy level and large electron energy barrier height was preferred [7]. In addition, it was reported that the traps of TPO could cause the charge loss to be increased and, thus, should be minimized [6,8].

In spite of such various approaches, there are not enough studies to understand the physical mechanisms, in particular, related to the amount of charge injection (ΔV_{TH}) and metal gate in terms of the data retention of the CTF memory. In this study, we investigated the retention characteristics of the $SiO_2/Si_3N_4/Al_2O_3$ (ONA) stack and the $SiO_2/Si_3N_4/SiO_2$ (ONO) stack at various levels of ΔV_{TH} as well as the impact of metal gate on the charge loss including its P/E speed.

2. Experimental method

For this study, we used ONA (=4 nm/7 nm/15 nm) stacks and ONO (=4 nm/5.5 nm/7.5 nm) stacks. Thermally grown SiO_2 was used for the BTO. A Si_3N_4 layer was deposited by low-pressure chemical vapor deposition (LPCVD) on the BTO for the storage of charges. As a TPO to block the charge loss, an Al_2O_3 layer was deposited by means of atomic layer deposition. More details regarding ONA stack formation are described in another publication [8]. For a comparison with ONO stack, we deposited a SiO_2 layer by means of LPCVD. TaN and Pt were deposited by means of RF sputter for the metal electrode and capping layer, respectively. For the metal gate study, we additionally prepared ONA stacks with 20 nm-Al and 20 nm-Pt metals, respectively. Al and Pt were deposited by e-beam. Subsequently, as a capping layer, 20 nm-Pt was deposited on the metal gate. Finally, forming gas annealing was performed at 400 °C for 30 min. In our study, the approximate Φ_M of Al and Pt was found to be 4.2 and 5.6 eV, respectively, extracting by the flat band voltage versus the equivalent oxide thickness plot [9].

3. Experimental results

For ease of understanding about the retention state of the device, Fig. 1 shows the energy band diagrams for the ONA stack at

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various levels of ΔV_{TH}. At an initial state (ΔV_{TH} = 0 V), it is certain that the tunneling distance across the BTO (d_{BTO}) is absolutely shorter than across the TPO (d_{TPO}). However, as ΔV_{TH} is gradually increased, d_{TPO} becomes more comparable to d_{BTO}. Finally, at a high level of programmed state (ΔV_{TH} = 8 V), it seems that d_{TPO} is shorter than d_{BTO}. From this figure, the amount of band bending across either BTO or TPO as a function of ΔV_{TH} and the variation of d_{BTO} and d_{TPO} for the electrons on the Si_3N_4 conduction band (CB) could be predicted. In here, we assumed that trap centroid (X_c) is located at a middle of Si_3N_4 thickness [10]. Thus, the internal electric field induced by ΔV_{TH} is divided by [11]:

$$\Delta V_{TH} = V_{BTO} + V_{X_c} = V_{Si_3N_4-X_c} + V_{TPO} \quad (1)$$

Further to voltage division, we can calculate both d_{BTO} and d_{TPO} according to Eq. (1). In this manner, we calculated the tunneling time constant (τ) for electrons thermally de-trapped into the Si_3N_4 CB ($1/e_{th}$) and then tunneled through the oxide ($1/e_{ox}$, BTO or TPO) using the following equation [12,13].

$$\tau = 1/e_{ox}e_{th} = 1/e_{ox,0}AT^2 \exp(-2d_{ox}\sqrt{2qm^*\Phi_{ox}}/\hbar - E_{TA}/kT) \quad (2)$$

where $e_{ox,0}$, A and T are the intrinsic time constant, temperature independent constant, and the retention temperature, respectively. d_{ox} is either d_{BTO} or d_{TPO}. m^* is the electron effective mass (m^* SiO_2 = 0.42, m^* Al_2O_3 = 0.2), Φ_{ox} is the energy barrier height for electron emission ($\Phi_{Al_2O_3}$ = 0.45 eV, Φ_{SiO_2} = 1.05 eV), E_{TA} is the trap energy level from the Si_3N_4 CB edge (1.4 eV in here). Compared to the $e_{th}e_{ox}$ of ONO symmetric stack (Fig. 2a), that of ONA asymmetric stack (Fig. 2b) has a specific critical point (~1.2 V) where the transition of dominant charge loss path is expected. Regarding to charge loss path, we believe that the BTO is dominant in the ΔV_{TH} range below 1.2 V while both the BTO and the TPO are dominant above 1.2 V.

To verify the theoretical results experimentally, we estimated the charge loss rate of ONO and ONA stacks with TaN metal (Fig. 3). $\Delta V_{FB,inj}$ indicates the difference of flat band voltage from the programmed state ($V_{FB,pgm}$) to initial state ($V_{FB,ini}$), that is, the amount of charge injection in MOS capacitor device. From Fig. 3, it is found that ONO stack exhibited a constant charge loss rate slope (γ) of 0.004 in the whole range of charge injection, while ONA stack showed two step γ (1st step = 0.001, 2nd step=0.016). Based on the results of Figs. 1 and 2, a constant slope means no transition of charge loss path (1st step, toward only BTO). Contrarily, 2nd step means the addition of charge loss path toward TPO to 1st step charge loss path. Unlike our expectation, there was a large discrepancy of critical point between the calculated value and the experimental one. This discrepancy arises because we still need other significant parameters for the band bending such as fixed charge [14], interfacial layer [15] and trap centroid [10,11].

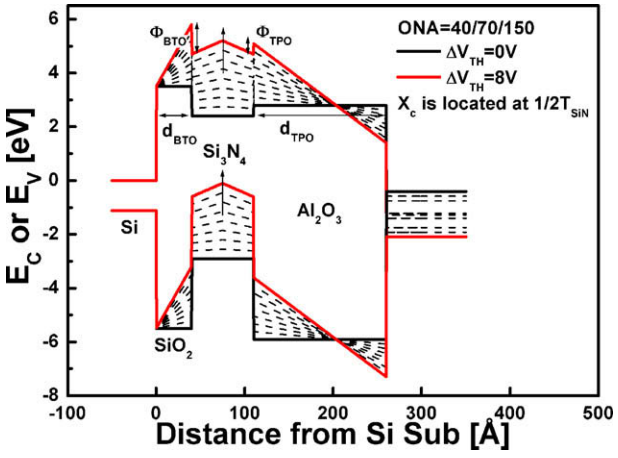

Fig. 1. Energy band diagrams for the ONA stack structure in retention state at various levels of charge injection.

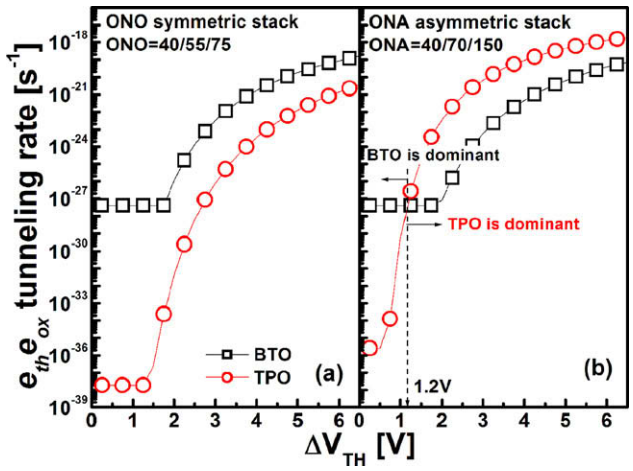

Fig. 2. Tunneling rates of $e_{th}e_{ox}$ for the ONO and ONA stacks.

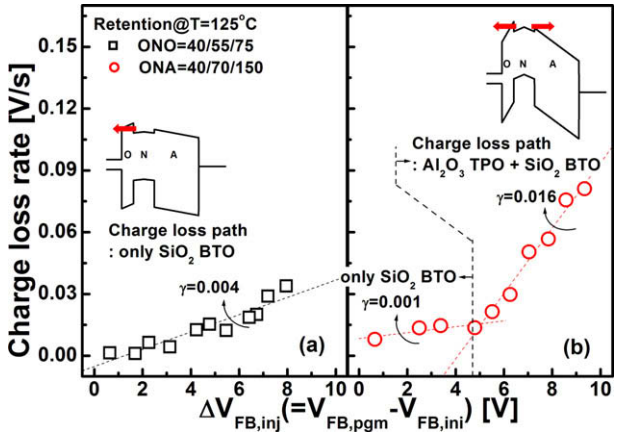

Fig. 3. Charge loss rate of ONO and ONA stacks with TaN metal at various levels of charge injection.

In the following, we investigated the impact of Φ_M on the P/E speed and data retentions at different programmed state. The ONA stack with Al and Pt metals showed similar program speed (Fig. 4a and b) although the difference of Φ_M could give them a little change of electric field across the ONA stack. It is well known that FN tunneling is closely related to the BTO thickness and barrier height (Si/SiO_2) rather than Φ_M [3]. However, in the case of erase speed (Fig. 4c and d), they showed significantly different erase behaviors. The ONA stacks with Al metal (n-type, low-Φ_M) exhibited poor erase characteristics due to the electron back tunneling (EBT, inset of Fig. 4c) from the gate [3]. On the contrary, the ONA stack with Pt (p-type, high-Φ_M) showed a good erase behavior. It is interesting to note that this EBT seems to be more dominant at the short pulse region (<10 ms) such that this gave rise to roll-up of V_{FB} shifts. This suggests that short-time erase pulses induce larger electron injection current from gate than hole current from substrate (or electron de-trapping). This related mechanism is still not completely understood.

For further studies, we measured charge loss rate at different program states, as shown in Fig. 5. Charge loss rate was extracted from retention data using linear fit. At the program state of 4 V, both metal samples shows almost same charge loss rate. On the other hand, charge loss rate of Al metal sample becomes larger

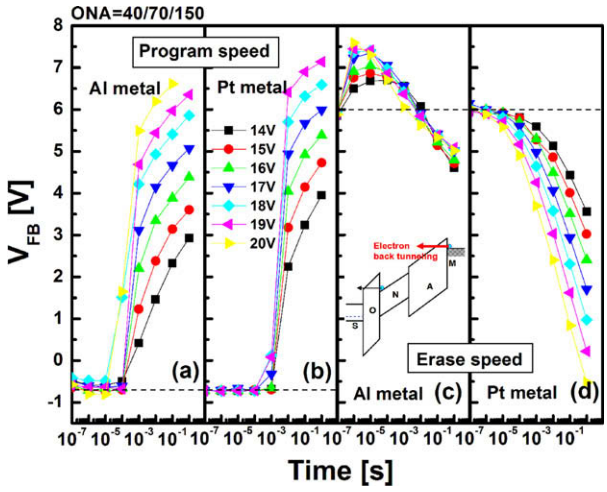

Fig. 4. P/E speed characteristics of ONA stacks with Al and Pt metals in the pulse amplitude range from ±14 V to ±20 V. Inset figure illustrates the energy band diagram of erase operation and EBT.

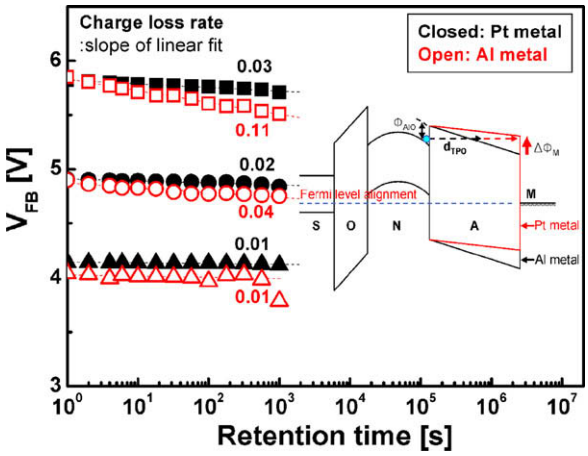

Fig. 5. Charge loss rates for the ONA stacks with different Φ_M of gate metals (Al and Pt) at different programmed state. Inset illustrates the energy band diagram with Fermi level alignment during retention characteristic.

than that of Pt metal with increasing program states. Considering the charge loss path at high level of programmed state (>4 V) (Fig. 3b), this strongly suggests that the TPO with high-Φ_M could suppress the charge loss through the TPO, indicating improved retention characteristics. This can be explained by Fermi level alignment [16]. Inset of Fig. 5 shows the energy band diagram of ONA stack with different Φ_M of gate metals (Al and Pt) with alignment. In the case of Pt metal, the electric field across the TPO could be compensated by the $\Delta\Phi_M$ ($\Phi_{Pt} - \Phi_{Al} = 1.4$ eV) due to Fermi level alignment. Thus, d_{TPO} of p-type metal sample might be more extended than that of n-type metal sample. However, it is noticeable that this compensation effect may not be effective at the low programmed state of 4 V, because the electric field across the TPO induced by low level of charge injection is not enough to tunnel out, even if there is $\Delta\Phi_M$.

4. Conclusions

Charge loss behavior of ONA stack is highly dependent on ΔV_{TH}. Particularly, for large ΔV_{TH}, the charge loss path toward Al_2O_3 should be considered due to the band bending effect. This result was experimentally and theoretically verified. We also investigated the impact of charge injection and metal gates (Al and Pt) on the data retention. Compared to low-Φ_M, ONA stack with high-Φ_M showed better data retention characteristics, even if ΔV_{TH} is high. This could be explained by Fermi level alignment, which compensated the electric field across the Al_2O_3 by the $\Delta\Phi_M$ ($\Phi_{Pt} - \Phi_{Al}$).

Acknowledgements

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