Electrical Properties of Surface-Tailored ZnO Nanowire Field-Effect Transistors

Woong-Ki Hong, Gunho Jo, Soon-Shin Kwon, Sunghoon Song, and Takhee Lee

(Invited Paper)

***Abstract*—A review on the tunable electrical properties of ZnO nanowire field-effect transistors (FETs) is presented. The FETs made from surface-tailored ZnO nanowire exhibit two different types of operation modes, which are distinguished as depletion and enhancement modes in terms of the polarity of the threshold voltage. We demonstrate that the transport properties of ZnO nanowire FETs are associated with the influence of nanowire size and surface roughness associated with the presence of surface trap states at the interfaces as well as the surface chemistry in environments.**

***Index Terms*—Field-effect transistor (FET), passivation, surface roughness, ZnO nanowire.**

I. Introduction

ONE-DIMENSIONAL single-crystalline nanostructures of semiconducting metal oxides such as ZnO [1], In_2O_3 [2], and SnO_2 [3] have been extensively studied due to their potential use for future nanoelectronic device applications. Among these, ZnO nanostructures have attracted considerable attention due to their unique properties such as direct wide band gap ($\sim$3.4 eV) and large exciton binding energy (60 meV) and their versatile applications such as field-effect transistors (FETs) [1], [4], [5], sensors [6]–[8], optoelectronic devices [9]–[11], solar cells [12], [13], and logic circuits [14]. In particular, since nanowire-based FETs are the fundamental element for nanoelectronics among these versatile applications, ZnO nanostructure-based FETs have been fabricated and extensively investigated in a typical back-gate configuration [1], [4], [5], [15], [16]. Such early studies of ZnO nanowire FETs have focused only on their device performance [15], [16], gas sensing application [6], [7], photodetection [10], [11], [17], and chemisorption/photodesorption [18], [19]. However, until now, there are not many studies on the role of geometric properties, surface states, and passivation on the transport properties of ZnO nanowire FETs, specifically on the influence of nanowire size and surface roughness associated with the presence of surface trap states at the interfaces. It is well known that interface roughness plays an important role in the electronic transport for transistors [20], [21], and in particular, the properties of nanostructures used as building blocks for the assembly of nanoscale devices strongly depend on their size and shape [22]–[25].

Therefore, it is essential to understand the surface-roughness- and size-dependent effects on the electronic transport properties of nanowire transistors. Moreover, since ZnO nanowires are strongly influenced by chemical environments [1], [6], [7], [18], [19], it is important to study on the passivation effects of the dielectric layer on the transport properties correlated to geometry and adsorbed species on the ZnO nanowires.

In this paper, we present the tunable electrical properties of FETs made from the surface-tailored ZnO nanowires that were grown on various substrates by a vapor transport method. We demonstrate that the transport properties of ZnO nanowire FETs are associated with the surface roughness of nanowires, nanowire size, and surface states and/or defects as well as the surface chemistry in environments. These explorations will give insights not only in understanding the transport properties but also in developing practically useful applications of nanowire-based devices.

II. Experimental Procedure

Surface-tailored ZnO nanowires having smooth and rough surface morphologies were grown on ZnO buffer-film-coated c-plane sapphire substrates with or without using Au catalysts by a vapor transport method. As it has been reported elsewhere in detail [26], the surface-tailored ZnO nanowires were grown on various substrates: 1) an undoped ZnO film with Au catalyst (denoted as Au–ZnO) or without Au catalyst (denoted as ZnO); 2) a gallium-doped ZnO film with Au catalyst (denoted as Au–GZO) or without Au catalyst (denoted as GZO); 3) an aluminum-doped ZnO film with Au catalyst (denoted as Au–AZO) or without Au catalyst (denoted as AZO); and 4) an Au-coated sapphire (denoted as Au–sapphire) substrate. The size, surface morphology, and crystal structure of the ZnO nanowires were characterized using field emission scanning electron microscopy (FESEM) and transmission electron microscopy (TEM). The average diameters of the ZnO nanowires were found to be approximately 84, 90, 86, 112, 108, 89,

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and 113 nm for the nanowires grown on Au–ZnO, ZnO, Au–GZO, GZO, Au–AZO, AZO, and Au–sapphire substrates, respectively. Here, the average diameter of each type of nanowire was determined statistically from FESEM images of roughly 100 different nanowires grown on each different type of substrate. The photoluminescence (PL) mapping system (RPM2000 model, Accent Opt. Tech., U.K.) with a 325-nm He–Cd laser (4.6 mW) as an excitation source was used to study the luminescence properties of the ZnO nanowires at room temperature. In particular, in order to eliminate signals coming from the ZnO buffer films themselves, ZnO nanowires were transferred from the growth substrates to silicon wafers, and the PL spectra were obtained from the ZnO nanowires transferred on silicon wafers. Note that the PL spectra were obtained from the average values of individual signals acquired from 13 different positions on each ZnO nanowire-transferred wafer. In addition, in order to perform statistical analysis of the electronic transport characteristics of surface-tailored ZnO nanowires, a total of 327 nanowire FET devices were fabricated and characterized: 48 FETs of nanowires grown on Au–ZnO, 41 FETs of nanowires grown on ZnO, 54 FETs of nanowires grown on Au–GZO, 55 FETs of nanowires grown on GZO, 58 FETs of nanowires grown on Au–AZO, 51 FETs of nanowires grown on AZO, and 59 FETs of nanowires grown on the Au–sapphire substrate. A detailed description of the fabrication of ZnO nanowire FET devices has been reported elsewhere [26]. These nanowire FET devices were passivated by poly(methyl methacrylate) (PMMA) to eliminate the influence of water or gas molecules in ambient air on ZnO nanowire FETs and to improve the FET performance by enhancing the gate-coupling effects. We also studied on the electrical properties of ZnO nanowire FET devices before and after PMMA passivation. The electronic transport characteristics of the ZnO nanowire FETs were investigated using a semiconductor parameter analyzer (HP4155C) at room temperature.

III. Results and Discussion

A. Structural and Optical Properties of ZnO Nanowires

The representative TEM images of surface-tailored ZnO nanowires are shown in Fig. 1. The low-magnification [Fig. 1(a) and (b)] and high-resolution TEM images [Fig. 1(c) and (d)] show two different types of ZnO nanowires, one with a smooth surface [Fig. 1(a) and (c)] and the other with a rough surface [Fig. 1(b) and (d)]. Insets of Fig. 1(c) and (d) are selected-area electron diffraction (SAED) patterns obtained from the lattice fringes of ZnO nanowires. These SAED patterns and other electron diffraction patterns taken from the entire nanowire structure (not shown here) indicate that both smooth and rough ZnO nanowires are single crystalline with a preferred growth direction of [0001] and corresponding lattice fringes of 0.52 nm. Moreover, no distinctive difference of crystal quality was found between the edges of the rough nanowires and those of the smooth nanowires. However, the degree of the surface roughness of the nanowires from these TEM images could be estimated in the following two ways: 1) the "absolute" roughness, which can be defined as the difference of the arithmetic

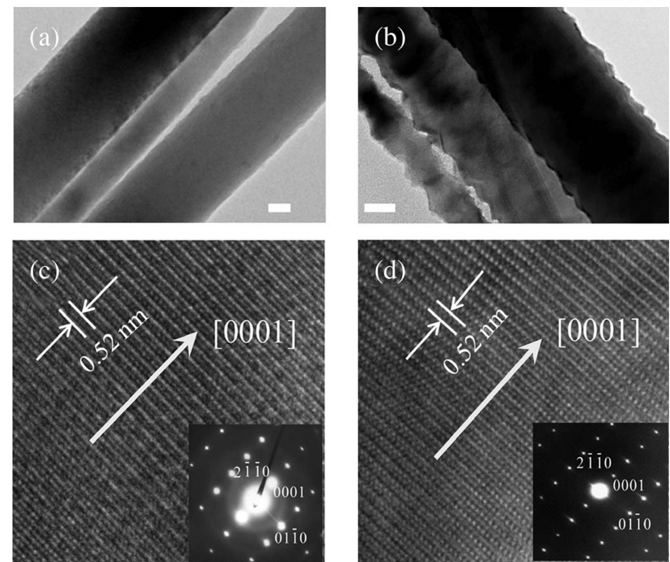

Fig. 1. Low-magnification TEM images of (a) smooth ZnO nanowire grown on Au–sapphire substrate and (b) rough ZnO nanowire grown on Au–GZO substrate. The scale bar is 20 nm. High-resolution TEM images of (c) smooth ZnO nanowire and (d) rough ZnO nanowire. Insets of (c) and (d) show SAED patterns.

mean values of the maximum and minimum diameters of the corrugated nanowires, and 2) the "relative" roughness, which can be defined as the absolute roughness divided by the average diameters of the rough nanowires. In these ways, we found the {absolute and relative roughness} as {6.4 nm and 7.7%}, {6.6 nm and 7.3%}, {7 nm and 8.2%}, and {5.8 nm and 6.5%} for the rough nanowires grown on Au–ZnO, ZnO, Au–GZO, and AZO, respectively. Although the size-dependent growth mechanism of ZnO nanowires with smooth and rough surfaces grown on different substrates is not yet clearly understood, ZnO nanowires with distinctive surface roughness and diameter size can be grown due to various effects, which include nanocatalyst composition [27], interfacial layer [28], surface charge [29], surface roughness [30], surface strain [30], tensile stress [31], and Zn supersaturation variation [32].

Fig. 2(a) shows the PL spectra measured at room temperature for two different types of ZnO nanowires grown on various substrates. As shown in Fig. 2(a), the PL emissions of both smooth and rough ZnO nanowires consist of two main bands; one is the near bandedge excitonic related ultraviolet (UV) emission band, and the other is the broad deep-level (DL)-related emission (or defect emission) in the visible range. The DL-related emission is determined by the surface states and/or the surface defects [33]–[37]. For the rough ZnO nanowires with relatively smaller diameters, the DL-related emission is strong and the UV emission becomes relatively weak, whereas for the smooth ZnO nanowires with relatively larger diameters, the DL-related emission is weak and the UV emission becomes relatively strong. Fig. 2(b) shows the relationship between the integrated intensity ratios of UV emission to DL-related emission $(I_{\mathrm{UV}}/I_{\mathrm{DL}})$ of the PL spectra of the ZnO nanowires [shown in Fig. 2(a)] and the nanowire diameter. Although the smooth and rough ZnO nanowires have both UV emission and DL-related emission peaks, the intensity ratios $I_{\mathrm{UV}}/I_{\mathrm{DL}}$ are

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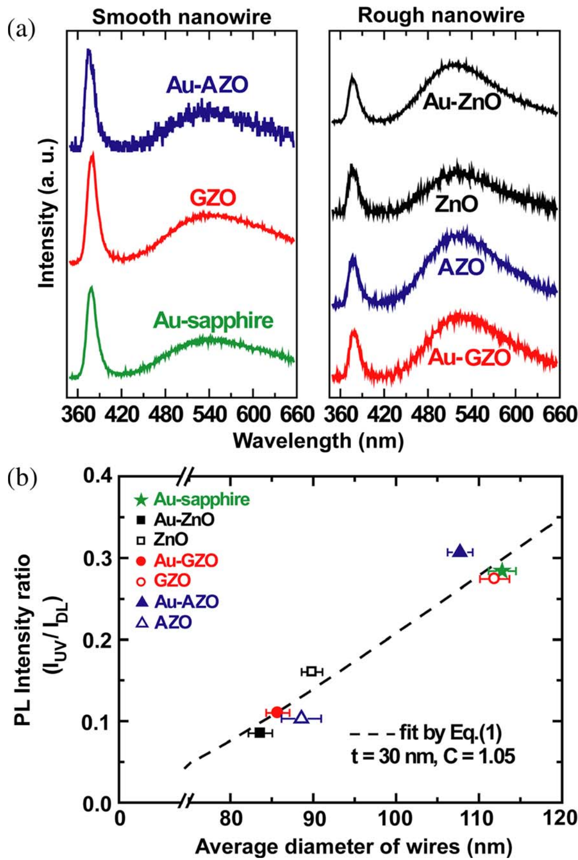

Fig. 2. (a) PL spectra of the ZnO nanowires grown on various substrates. (b) PL intensity ratios $I_{\mathrm{UV}}/I_{\mathrm{DL}}$ with a fitting curve as a function of the average diameter of ZnO nanowires.

very different between rough and smooth ZnO nanowires, as shown in Fig. 2(b). Smooth ZnO nanowires with relatively larger diameters exhibited larger $I_{\mathrm{UV}}/I_{\mathrm{DL}}$ ratios than rough ZnO nanowires with relatively smaller diameters. Since the DL-related emission is a surface-related process, it reveals that the ZnO nanowires with large $I_{\mathrm{UV}}/I_{\mathrm{DL}}$ ratios have a low density of surface states and/or defects, whereas those with small $I_{\mathrm{UV}}/I_{\mathrm{DL}}$ ratios have a high density of surface states and/or defects [33]–[37]. Therefore, the PL spectra and the $I_{\mathrm{UV}}/I_{\mathrm{DL}}$ ratios are influenced by the surface effects and the diameter size of nanowires. The $I_{\mathrm{UV}}/I_{\mathrm{DL}}$ ratios can be fitted using the surface-recombination-layer approximation model with the following [33]:

$$\frac{I_{\mathrm{UV}}}{I_{\mathrm{DL}}} = C\left(\frac{(D/2)^2}{2(D/2)t - t^2} - 1\right) \tag{1}$$

where C is an approximation constant related to a collection efficiency difference at wavelengths of UV emission and DL-related emission peaks, D is the nanowire diameter, and t is a surface recombination thickness [33]. The thickness of the surface recombination layer (t) was assumed to be 30 nm as the previously reported value [15], [38]. The optimized fitting curve obtained with (1) (using $t = 30$ nm and $C = 1.05$) is plotted as the dashed line in Fig. 2(b). This result implies that the contribution of the surface recombination to DL-related emission is predominant for smaller diameter nanowires, resulting in the increased surface effects [15], [34]–[37]. Moreover, according to the analysis of X-ray absorption near-edge structure spectra of the ZnO nanorods by Chiou *et al.* [39], the effect of surface states is enhanced when the diameter of ZnO nanorods is decreased. Therefore, the luminescence of ZnO nanowires is dependent on the surface roughness and the diameter size of nanowires, which indicates that the surface roughness and size of nanowires play an important role in the process leading to visible emission. Although the origin of broad visible emission as typical characteristics of ZnO materials is still controversial, the surface states and/or defects are responsible for the surface-roughness- and size-dependent luminescence [15], [34]–[37]. These surface states and/or defects of ZnO materials can also introduce various defect energy levels inside the band gap of ZnO [40]–[44], so that the surface effects by such surface states and/or defects can influence the ZnO nanowire-based devices.

B. Electrical Properties of Surface-Tailored ZnO Nanowire FETs

In order to study the influence of surface states and/or defects on the electrical properties of surface-tailored ZnO nanowires, we have examined the electrical characteristics using the nanowire FETs fabricated as a typical back-gated configuration. The electrical characteristics of ZnO nanowire FETs are shown in Figs. 3–5. Note that all the fabricated ZnO nanowire FETs were passivated by PMMA because ZnO nanowires are significantly affected by water or gas molecules in ambient air [45]–[47]. Fig. 3(a) and (b) shows the representative data of output characteristics (source–drain current versus voltage, I_{DS}–V_{DS}) and also transfer characteristics (source–drain current versus gate voltages, I_{DS}–V_G), respectively, for an n-channel depletion-mode FET made from smooth ZnO nanowires. Moreover, Fig. 3(c) and (d) shows I_{DS}–V_{DS} and $I_{\mathrm{DS}}V_G$ characteristics, respectively, for an n-channel enhancement-mode FET made from rough ZnO nanowires. Both smooth and rough ZnO nanowires show typical n-type semiconductor behavior, which is due to intrinsic donor-type defects induced by deviations from stoichiometry [48], [49]. The I_{DS}–V_G curve in Fig. 3(b) shows that the FET devices of smooth ZnO nanowires are in normally on-type n-channel depletion mode, which exhibits nonzero current at zero gate bias and negative threshold voltages [50]. On the contrary, FET devices made from rough ZnO nanowires show normally off-type n-channel enhancement-mode behavior, which has off-current status at zero gate bias and positive threshold voltages [50]. Both I_{DS}–V_{DS} curves [Fig. 3(a) and (c)] show well-defined linear regions at low biases and saturation regions at high biases. This is in good agreement with the characteristics of ZnO nanobelt FETs with Ti/Au ohmic contacts [51]. The I_{DS}–V_G curve [Fig. 3(b)] shows that the threshold voltage V_{th} is -2.96 V for depletion-mode FET, whereas the I_{DS}–V_G curve [Fig. 3(d)] shows that the threshold voltage V_{th} is 8.51 V for enhancement-mode FET. The I_{DS}–V_G plots in the semilogarithmic scale [insets of Figs. 3(b) and (d)] display an on/off current ratio as large as 10^5–10^6. The negative threshold voltage is attributed to delocalized electrons from

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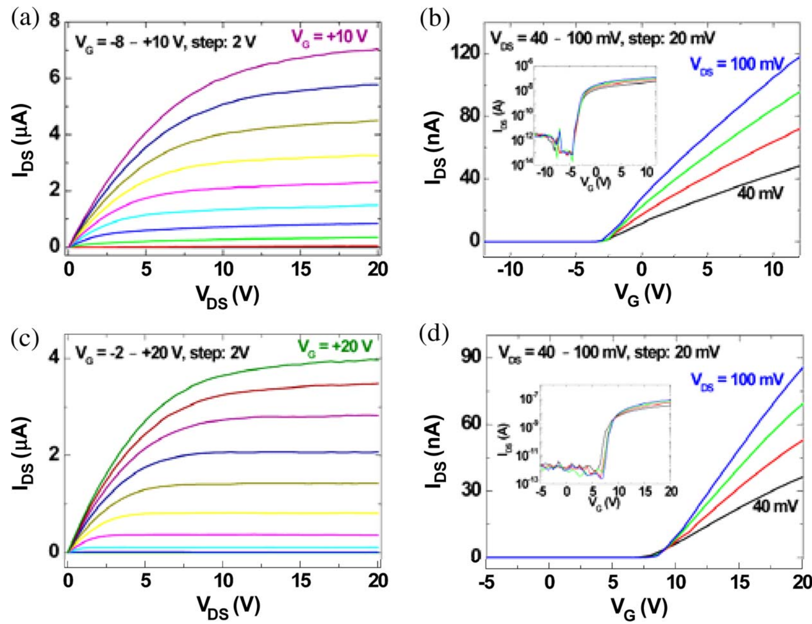

Fig. 3. I_{DS}–V_{DS} and I_{DS}–V_G curves for [(a) and (b)] n-channel depletion-mode FET of smooth ZnO nanowire and [(c) and (d)] n-channel enhancement-mode FET of rough ZnO nanowire. The insets of (b) and (d) show the semilogarithmic plots of the I_{DS}–V_G curves displaying on/off current ratios as large as 10^5–10^6.

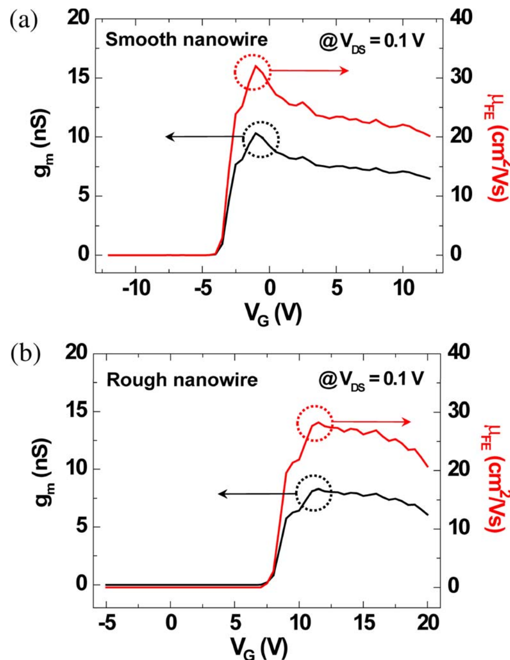

Fig. 4. Transconductance (g_m) and field-effect mobility (μ_{FE}) as a function of gate bias at $V_{\mathrm{DS}} = 0.1$ V for (a) FET of smooth ZnO nanowire and (b) FET of rough ZnO nanowire.

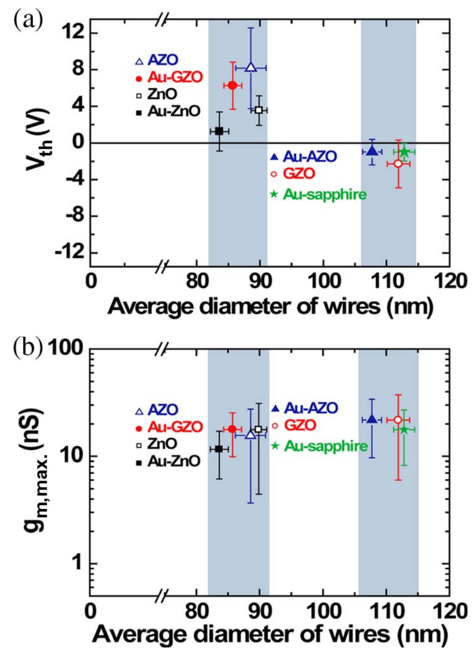

Fig. 5. (a) Distribution of threshold voltages (V_{th}) and (b) maximum transconductances ($g_{m,\max}$) as a function of the average diameter of ZnO nanowires.

shallow donors in the channel [Fig. 3(b)], whereas the positive threshold voltage is attributed to deep traps in the channel or at the interface [Fig. 3(d)] [52]. Therefore, the electrical properties of the smooth ZnO nanowires with relatively larger diameters are quite different from those of the rough ZnO nanowires with relatively smaller diameters due to the scattering or trapping of the conduction electrons at the interfaces and/or near the surface of the ZnO nanowire. Note that the threshold voltage is defined as the gate voltage obtained by extrapolating the linear portion of the transfer characteristics I_{DS}–V_G from the point of maximum slope to zero drain current, in which the point of maximum slope is the point where transconductance ($g_m = dI_{\mathrm{DS}}/dV_G$) is maximal [53].

Fig. 4(a) and (b) shows the plots of the corresponding transconductance ($g_m = dI_{\mathrm{DS}}/dV_G$) curves obtained from transfer characteristics I_{DS}–V_G and the calculated mobility as a function of gate voltage for n-channel depletion- (smooth nanowire) and enhancement-mode (rough nanowire) FETs, respectively. The carrier mobility in the low field region is then related to the transconductance mobility, also called the

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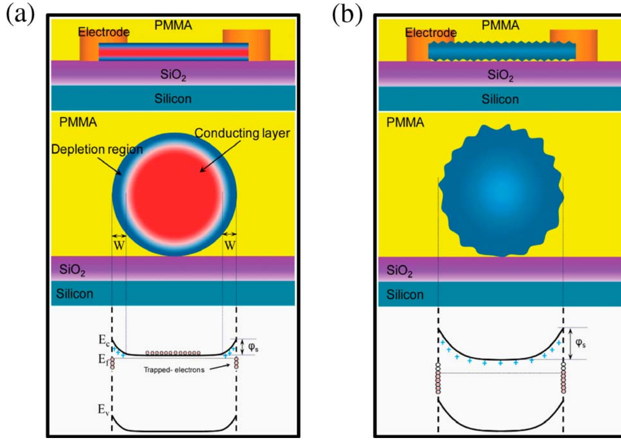

Fig. 6. (Top) Cross-sectional schematics across the electrodes, ZnO nanowire, and dielectric layers, and (bottom) the corresponding equilibrium energy band diagrams of nanowire FETs at $V_G = 0$ V for (a) smooth and (b) rough ZnO nanowires.

field-effect mobility (μ_{FE}). The field-effect mobility can be calculated by the following:

$$\mu_{\mathrm{FE}} = \frac{dI_{\mathrm{DS}}}{dV_G}\frac{L^2}{V_{\mathrm{DS}}C_G} \tag{2}$$

$$C_G = \frac{2\pi\varepsilon_r\varepsilon_0 L}{\cosh^{-1}\left(\frac{r+h}{r}\right)} \tag{3}$$

where C_G is the gate-nanowire capacitance, h is the gate oxide thickness $(= 100$ nm), r is the nanowire radius, ε_r is the dielectric constant of the gate insulating layer ($\varepsilon_r = 3.9$ for SiO_2), ε_0 is the permittivity constant of vacuum, L is the nanowire channel length (~ 4 μm), and $V_{\mathrm{DS}} = 0.1$ V.

Fig. 5(a) and (b) shows the distribution of threshold voltages and the maximum transconductance versus average diameter of ZnO nanowires grown on various substrates, respectively. For the statistical analysis on the electrical characteristics of the surface-tailored ZnO nanowire FETs, we examined all 327 FETs of the ZnO nanowires grown on various substrates. As shown in Fig. 5(a), the smooth ZnO nanowires with relatively larger diameters have negative threshold voltages, exhibiting depletion-mode behavior, whereas rough ZnO nanowires with relatively smaller diameters have positive threshold voltages, exhibiting enhancement-mode behavior. This result indicates that the surface roughness and the diameter size of nanowires can have a significant influence on the operation mode of nanowire-based FET devices. In addition, the maximum transconductance above threshold voltage does not quite depend on the nanowire diameter and the surface roughness in our back-gate ZnO nanowire FETs as shown in Fig. 5(b).

The mechanism of different operation modes in relation with surface roughness, which is associated with the presence of surface trap states at the interfaces, is shown in Fig. 6. Fig. 6 shows the cross-sectional schematics [top figures in Fig. 6(a) and (b)] across the electrodes, ZnO nanowire, and dielectric layers with the corresponding equilibrium energy band diagram [bottom figures in Fig. 6(a) and (b)] of the ZnO nanowire FETs at $V_G = 0$ V. Fig. 6(a) shows the case for smooth ZnO nanowire FETs, and Fig. 6(b) shows the case for rough ZnO nanowire FETs. For polycrystalline and single crystalline semiconductor materials, surface band bending can occur at grain boundaries and interfaces due to interfacial traps or potential [21], [54]–[61]. Therefore, the surface states and/or defects on single crystalline nanowires can act as trap sites at the interfaces, resulting in surface band bending due to Fermi level pinning [23], [59], [62], [63]. The carrier trap states at the interfaces are important in determining the operation modes of transistors [52]. The trapping of carrier electrons in the trap states can cause electron depletion in the channel, resulting in a gate threshold voltage shift and a conductance modulation. In particular, rough ZnO nanowires with relatively smaller diameters can have a more significant fraction of the surface depletion region in the nanowire channel due to electron traps in comparison with smooth ZnO nanowires.

Correspondingly, the tunable electrical properties of surface-tailored ZnO nanowire FETs can be explained by considering the surface band bending due to depletion of electron carriers at the PMMA/ZnO nanowire and/or ZnO nanowire/SiO_2 interfaces. Note that, for convenience of discussion and simplification of charge transport mechanism, we assumed the uniform charge and gate potential distribution for ZnO nanowires with circular cross sections. Considering depletion region (W) by surface band bending at the interfaces of SiO_2/ZnO nanowire/PMMA, we can compare the geometrical diameter (D) with the nanowire effective diameter (D_{eff}) by using the depletion approximation and charge neutrality condition [1], [55], [62], [64], [65], which can be estimated as

$$W = \sqrt{\frac{2\varepsilon_{\mathrm{ZnO}}\varphi_S}{eN_D}} \tag{4}$$

$$N_t = 2N_D W \tag{5}$$

$$D_{\mathrm{eff}} = D - 2\sqrt{\frac{2\varepsilon_{\mathrm{ZnO}}\varphi_S}{eN_D}} = D - \left(\frac{N_t}{N_D}\right) \tag{6}$$

where φ_S is the surface barrier potential, e is the electronic charge, N_D is the doping density, $\varepsilon_{\mathrm{ZnO}}$ is the dielectric constant of ZnO, and N_t is the surface trap density. For example, by assuming that the $N_D = 10^{17}/\mathrm{cm}^3$, $\varepsilon_{\mathrm{ZnO}} = 8.66$ [67], and $\varphi_S = 0.3$ eV, we obtain $W = 54$ nm and $D < 2W$ from (4)–(6). This indicates that the surface depletion can have a significant influence on the electronic transport behavior of ZnO nanowire FETs since the surface depletion width can be comparable to the diameter size of nanowire. Therefore, smooth ZnO nanowires can be partially depleted under the no-gate-bias condition due to the smaller depletion region than the nanowire diameter [Fig. 6(a)], whereas rough ZnO nanowires can be completely depleted under the no-gate-bias condition [Fig. 6(b)] due to the larger depletion region than the nanowire diameter. This explains why the operation mode of ZnO nanowire FETs can be controlled by the modulation of surface states and/or defects by surface roughness and diameter size control. As a result, the smooth ZnO nanowire FETs with relatively larger diameters can operate in the n-channel

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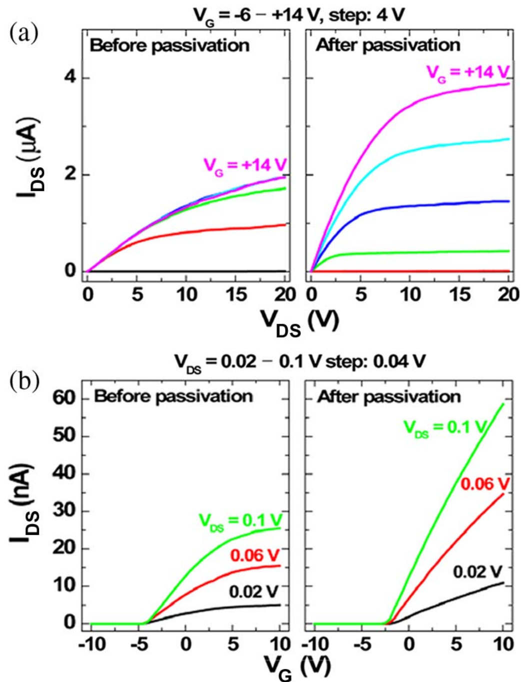

Fig. 7. (a) I_{DS}–$V_{\mathrm{DS}}$and (b) I_{DS}–V_G curves of a FET device made from smooth ZnO nanowires before and after passivation.

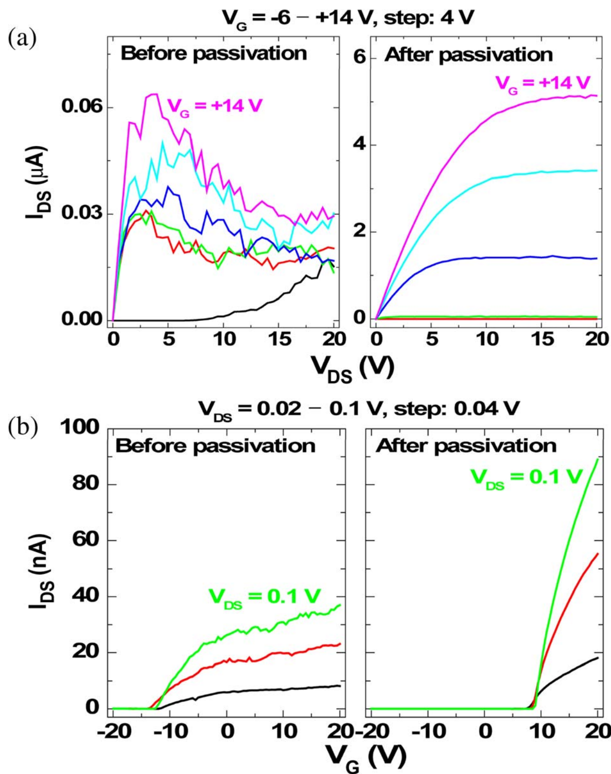

Fig. 8. (a) I_{DS}–V_{DS} and (b) I_{DS}–V_G curves of a FET device made from rough ZnO nanowires before and after passivation.

depletion-mode behavior with a partially depleted channel region [Fig. 6(a)], whereas the rough ZnO nanowire FETs with relatively smaller diameters can operate in the n-channel enhancement-mode behavior with a fully depleted channel region [Fig. 6(b)] under the no-gate-bias condition.

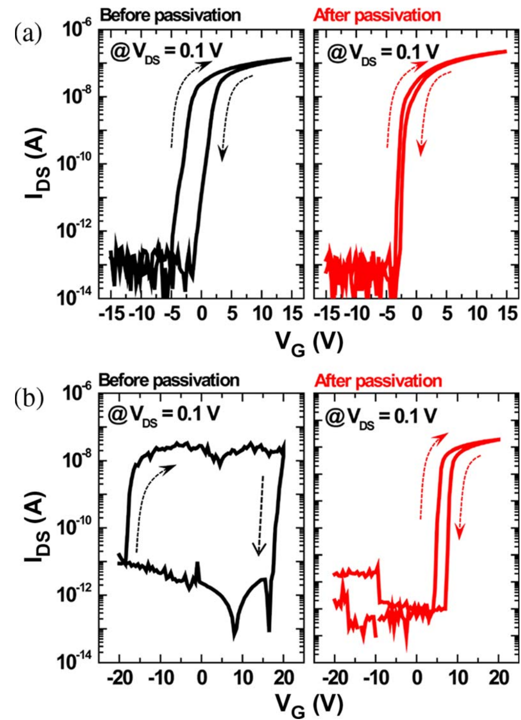

Fig. 9. Hysteresis behaviors for FET devices made from (a) smooth and (b) rough ZnO nanowires before and after passivation (at $V_{\mathrm{DS}} = 0.1$ V). The arrows show the direction of the gate voltage sweep.

C. Comparison of the Electrical Properties Before and After Passivation

The electrical characteristics before and after passivation of the FET devices made from smooth and rough ZnO nanowires are shown in Figs. 7–10. Note that, here, we have investigated the electrical properties of smooth and rough ZnO nanowires grown on Au–sapphire and Au–GZO substrates, respectively. Fig. 7(a) and (b) shows the representative I_{DS}–V_{DS} and I_{DS}–V_G characteristics for a FET made from smooth ZnO nanowires. As shown in Fig. 7(a), the FETs made from smooth ZnO nanowires exhibit more well-defined saturation and pinch-off characteristics after passivation in comparison with the FET devices before passivation. In particular, the unpassivated FET devices show the decreasing separation in current between I_{DS} curves at larger currents in I_{DS}–V_{DS} curves [Fig. 7(a)], which is attributed to either an electron injection barrier at the source electrode or to mobility degradation associated with the interface roughness scattering of channel electrons at the channel/insulator interface with increasing gate voltage [52]. The I_{DS}–V_G curves in Fig. 7(b) show the threshold voltages (V_{th}) of -4.16 and -2.25 V before and after passivation, respectively. Although the I_{DS}–V_G curves in all the fabricated FET devices were not shown here, the threshold voltages after passivation shifted toward the positive gate bias direction due to the surface-depletion-induced channel narrowing effect [46], [67]–[69]. However, regardless of the threshold voltage shift, most devices both before and after passivation operated in n-channel depletion mode [Fig. 7(b)]. The current on/off ratios $(I_{\mathrm{on}}/I_{\mathrm{off}})$ before and after passivation for this FET device of smooth ZnO nanowire exhibited 10^4–10^5.

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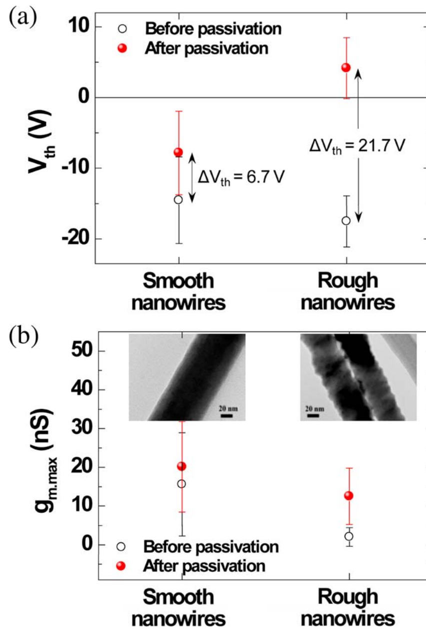

Fig. 10. Comparison of (a) threshold voltage ($V_{\rm th}$) and (b) maximum transconductance ($g_{m,\max}$) of the FET devices made from smooth and rough nanowires before and after passivation. The insets show smooth and rough ZnO nanowires grown on Au–sapphire and Au–GZO substrates, respectively. A total of 44 ZnO nanowire FET devices were fabricated and measured (22 FETs of smooth ZnO nanowires and 22 FETs of rough ZnO nanowires).

For the FET devices made from rough ZnO nanowires, the unpassivated devices exhibited poor electrical characteristics, as the representative $I_{\rm DS}$–$V_{\rm DS}$ data shown in Fig. 8(a). The $I_{\rm DS}$ suddenly decreased with the further increase of $V_{\rm DS}$ and V_G beyond saturation, and also, the separation in current between $I_{\rm DS}$ curves was not clear. In contrast, the passivated devices exhibited well-defined linear regions at low biases and saturation regions at high biases as typical transistors, indicating clear pinch-off behavior. Unlike the FET devices made from smooth ZnO nanowires, the threshold voltages for the FET devices made from rough ZnO nanowires exhibited a considerable shift toward the positive gate bias direction after passivation. The threshold voltage of the particular FET device shown in Fig. 8(b) shifted from -12.5 to 8.9 V, indicating transition from depletion- to enhancement-mode operations. Similarly, most of the passivated FET devices of rough ZnO nanowires exhibited superior electrical performance than the unpassivated devices of rough ZnO nanowires. These results are in good agreement with the superior characteristics of the ZnO nanowire FETs passivated by $\rm SiO_2/Si_3N_4$ or PMMA layer [16], [45], [70]. The current on/off ratios $(I_{\rm on}/I_{\rm off})$ before and after passivation for the FET device of rough ZnO nanowire exhibited approximately 10^4-10^5.

Fig. 9(a) and (b) shows the hysteretic behavior before and after passivation of FET devices made from smooth and rough ZnO nanowires, respectively. The hysteresis width for the unpassivated FET device of the smooth ZnO nanowires is much smaller than that for the rough ZnO nanowires. Moreover, the unpassivated ZnO nanowire FETs exposed to ambient air showed a strong hysteresis behavior, whereas the PMMA-passivated devices showed the considerable reduction of the undesired hysteresis. These results indicate that the hysteresis of ZnO nanowire FETs depend on chemical environments. It has been already reported by Goldberger *et al.* [1] that the presence of adsorbed species on or near the ZnO nanowires plays a significant role in the hysteresis of ZnO nanowire FETs. In particular, the rough ZnO nanowires have high density of surface states (Fig. 2), and thus, they can have much more adsorbed sites on nanowire surface than the smooth ZnO nanowires. Ultimately, the hysteretic behavior can be caused by traps located along the gate oxide/ZnO nanowire/air ambient interfaces [1]. For example, charge trapping by the adsorbed water molecules can be an important cause of the hysteresis in ZnO nanowire FETs exposed to air ambient. This is consistent with the hysteresis caused by water molecules in carbon nanotube FETs [71].

Fig. 10 shows the statistical results of the changes in the threshold voltages and the transconductances before and after the passivation of a total of 44 ZnO nanowire FET devices characterized as follows: 22 FET devices of smooth ZnO nanowires and 22 FET devices of rough ZnO nanowires. For the FETs made from smooth ZnO nanowires, the average shift in threshold voltage $(\Delta V_{\rm th})$ is around 6.7 V, whereas the $\Delta V_{\rm th}$ for those of rough ZnO nanowires is 21.7 V, as shown in Fig. 10(a). The threshold voltages in the FET devices of both of these two types of ZnO nanowires shifted toward the positive gate bias direction, implying the surface-depletion-induced channel narrowing due to the presence of electron traps of the ZnO nanowire [46], [67]–[69]. In particular, the FETs made from rough ZnO nanowires showed the depletion-mode behaviors before passivation and enhancement-mode behaviors after passivation. Furthermore, the changes in the threshold voltages for the rough ZnO nanowires were much more dramatic than those for the smooth ZnO nanowires. These results indicate that the surface roughness of ZnO nanowires causes the threshold voltage to shift toward the positive gate bias direction because the channel width is narrowed due to the aforementioned formation of a significant surface depletion region by the trap of electrons at ZnO nanowire/$\rm SiO_2$ and/or ZnO nanowire/PMMA interfaces. This is consistent with the shifts in the threshold voltage due to the channel narrowing effect by surface band bending at the interfaces of the ZnO nanowire/oxygen molecules and the Au/CdS nanobelt Schottky contact [46], [67]. Moreover, for the passivated ZnO nanowire FET devices, the significant shifts in threshold voltages of rough ZnO nanowires can be attributed to the increased scattering effect and deep traps of channel electrons at the interfaces, i.e., at the electrodes/ZnO nanowire and at the ZnO nanowire/insulating layers. In particular, the rough ZnO nanowires have a larger surface area to volume ratio than the smooth ZnO nanowires, and thus, the surface depletion region due to the trap of electrons at the interfaces will occupy a more significant fraction of the ZnO nanowires with smaller diameters than those with larger diameters.

In addition, in both types of ZnO nanowires, the transconductance of the passivated FETs increased than that for the unpassivated devices [Fig. 10(b)], indicating more efficient gating effects after passivation, which is consistent with the electrical characteristics of back-gate ZnO nanowire FETs by $\rm SiO_2/Si_3N_4$ passivation [16] and top-gate ZnO nanorod MOSFETs [72]. Most of the unpassivated FET devices of

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the rough ZnO nanowires showed weaker gate dependence than those of the smooth ZnO nanowires, implying weaker electrostatic gating effects and much lower capacitances for the rough ZnO nanowires. The inferior electrical characteristics of the rough ZnO nanowire-based FETs without the passivation layer can also be due to the weak gate coupling caused by the physically poor contact between the nanowire and the SiO_2 layer. However, after passivation by the PMMA layer, nanowires are embedded within the insulating layer, leading to the enhancement of the gating effects and transconductance. For example, Wunnicke [73] has reported that the capacitance of the nonembedded nanowire FETs is nearly half of that for the embedded nanowire FETs. Thus, the passivated FETs have larger transconductance than the unpassivated devices, implying the stronger electrostatic gating effects for the FETs after passivation.

IV. Conclusion

We presented the tunable electrical properties of the FET devices made from surface-tailored ZnO nanowires having different surface roughnesses and sizes. The electronic transport characteristics are significantly influenced by the nanowire size and surface roughness associated with the traps at the interfaces as well as surface chemistry environments. The characteristics show that the controlled optimum surface effects can lead to electrical tunability and wide applications of nanowires and the robust passivation of ZnO nanowire-based devices is important for practically useful nanoelectronic applications.

In the field of nanowire-based electronics, these explorations will give insights not only in clearly understanding the transport behavior but also in developing practically useful applications of nanowire-based devices.

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