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Electrical properties of ZnO nanowire field effect transistors by surface passivation

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Abstract

We have synthesized single crystalline ZnO nanowires by thermal evaporation method and fabricated individual ZnO nanowire field effect transistors (FETs) to investigate their electrical properties. ZnO nanowires are strongly affected by O_2 molecules in ambient. For example, surface defects such as oxygen vacancies act as adsorption sites of O_2 molecules, and the chemisorption of O_2 molecules depletes the surface electron states and reduces the channel conductivity. Therefore, it is important to protect the electrical properties of ZnO nanowires by surface passivation. For this purpose, we investigated the changes of the electrical properties of ZnO nanowire FETs with and without passivation by an organic material, poly(methyl metahacrylate) (PMMA). The ZnO nanowire FETs with PMMA passivation exhibited better performance in comparison with unpassivated devices.

Keywords: Passivation; ZnO; Nanowire; Field effect transistor; Nanoelectronics

1. Introduction

In recent years, one-dimensional semiconductor nanowires have been extensively studied due to their potential applications as building blocks for nanoelectronics, optoelectronics, electrochemical and sensor devices. Various semiconducting nanowires of single elements, compound semiconductors, and metal oxides have been successfully synthesized and studied [1–3]. Among these, ZnO nanowires are promising materials for nanoscale devices such as ultraviolet lasers, light-emitting diodes, photodetectors, chemical sensors, and solar cells since ZnO is direct wide-bandgap (3.37 eV) semiconductor with large exciton binding energy (60 meV) [4–8]. In particular, the electronic properties of semiconductor surfaces are strongly affected by the chemical adsorption (chemisorption) of ambient gases [9–14]. For example, it is well known that chemisorption of ambient gases, primarily oxygen, has a strong effect on the electrical properties of ZnO [15–19]. Therefore, it is particularly important to modify and protect the optoelectronic properties of ZnO nanowires against surface-mediated chemisorption by surface defect sites.

Recently, Fan et al. [20] have observed that the partial pressure of ambient oxygen has a considerable effect on the performance of ZnO nanowire field effect transistors (FETs). They have reported that the conductivity changes mainly due to the surface band bending, induced by O_2 molecule adsorption. The oxygen molecules absorbed at the defect sites of ZnO nanowires act as electron acceptors to form O_2^- at room temperature [21]. These chemisorbed O_2^- sites deplete the surface electron states and consequently reduce the channel conductivity. Also, there have been a few studies on the effect of surface passivation on ZnO nanowire FETs. [22–24]. For example, Chang et al. [22] have reported that ZnO nanowire FETs exhibit higher performance after passivation of the surfaces of the nanowires with a SiO_2/Si_3N_4 bilayer. However, the comparison of electrical properties such as carrier concentration and mobility with and without passivation has not been explored in detail. In this study, we report the electrical properties of ZnO nanowire FETs with and without passivation by poly(methyl metahacrylate) (PMMA). The single crystalline ZnO nanowires

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were grown by thermal evaporation and structural properties of the grown ZnO nanowires were studied with various analysis techniques. Then, the ZnO nanowires were fabricated into individual nanowire FET devices, and subsequently the transistor properties were investigated. For the surface passivation, the ZnO nanowire FET devices were coated by PMMA which is a polymeric resist commonly used in nanolithographic processes involving, for example, electron beam, deep UV (wave length of 220–250 nm), or X-ray radiation.

2. Experiment

ZnO nanowires were synthesized by thermally vaporizing a mixed source of commercial ZnO powder (99.995%) and graphite powder (99%) with a ratio of 1:1 in horizontal tube furnace. The *c*-plane sapphire was used as the substrates for nanowires growth. After cleaning the substrates, a layer of Au thin film (∼3 nm) was deposited on *c*-plane sapphire substrate with an electron beam evaporator. The source materials and Au deposited substrate were placed in an alumina boat, and then loaded at the center of the quartz tube. Then, the ZnO nanowires were grown on the Au-coated sapphire substrates at temperature of ∼920 °C for 20 min under the flow of a mixture of Ar and O_2 (0.2% O_2 in Ar) with a flow rate ∼50 sccm. The morphology of the ZnO nanowires grown on sapphire substrate was characterized using field emission scanning electron microscopy (FESEM). High resolution transmission electron microscopy (HRTEM) was used to confirm that the nanowires were single crystals. Photoluminescence (PL) spectrum was measured using a He–Cd laser (325 nm) as excitation source.

To fabricate the ZnO nanowire FET devices, ZnO nanowires grown on the sapphire substrate were transferred from the substrate to the silicon wafer with 100 nm thick thermally grown oxide by dropping a nanowire suspension in ethanol. The nanowire suspension was made by briefly sonicating the substrate with ZnO nanowires on its surface in the ethanol for

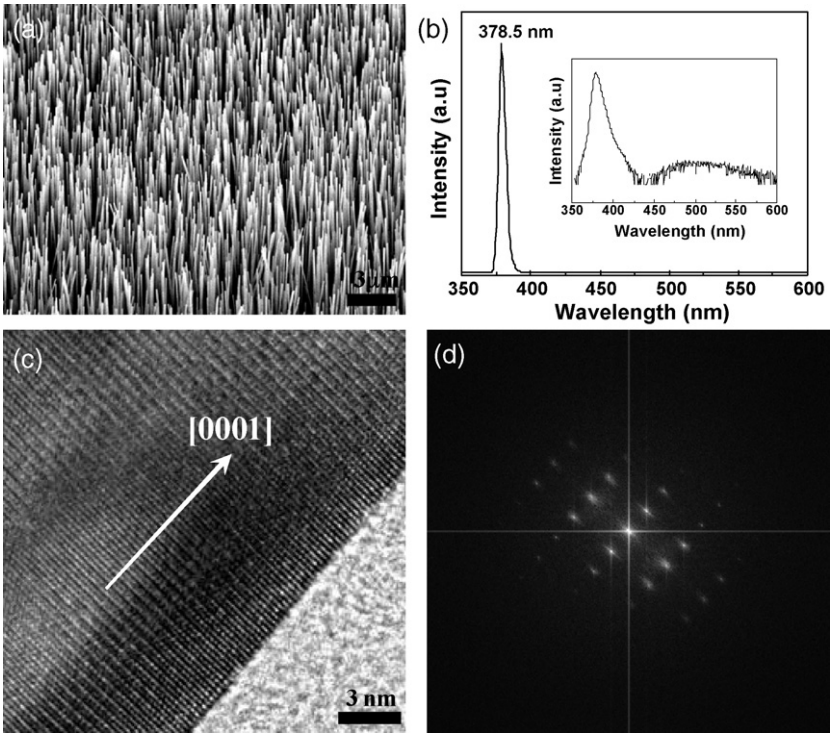

Fig. 1. (a) FESEM image (tilted view) of the ZnO nanowires grown on the sapphire substrate. (b) PL emission spectrum showing a strong emission at approximately 378.5 nm. The inset shows the logarithmic-scale plot. (c) HRTEM image of an individual ZnO nanowire showing its [0 0 0 1] growth direction. (d) The faster Fourier transform pattern corresponding to the lattice fringes from the nanowires.

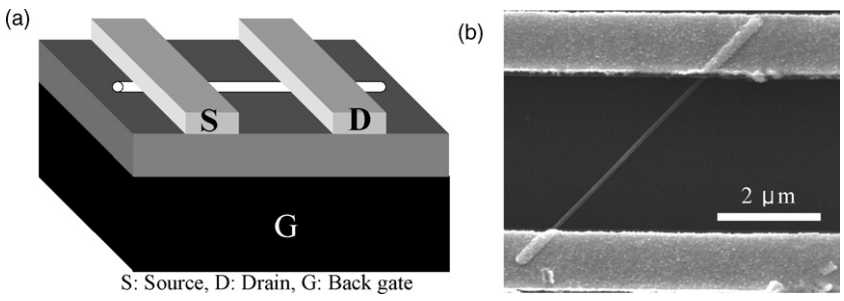

Fig. 2. (a) Schematic structure of ZnO nanowire FET. (b) FESEM image of ZnO nanowire FET.

30–60 s. The silicon wafers used in this study are a highly doped p-type substrate which can serve as a back gate electrode. Metal electrodes consisting of Ti (100 nm)/Au (100 nm) were deposited by an electron beam evaporator and defined as source and drain electrodes by a photolithography and lift-off process. The distance between source and drain electrodes is 3–4 μm. To compare the electrical properties of ZnO nanowire FETs with and without passivation, the fabricated devices were coated with PMMA 950 A4 (MicroChem) layer by spin coating with the speed of 4000 rpm, followed by soft-baking in oven at 90 °C for 10 min. After spin coating of PMMA layer, its thickness was found as around 200 nm from FESEM study. PMMA, which is a polymeric resist commonly used in nanolithographic processes such as electron beam, deep UV (wavelength of 220–250 nm) or X-ray radiation, exhibits thermal and mechanical stability, together with a high resistivity (>2×10^{15} Ω cm) and suitable dielectric constant, similar to that of silicon dioxide ($\varepsilon = 2.6$ at 1 MHz, $\varepsilon = 3.9$ at 60 Hz) [25]. Besides, PMMA can be easily deposited on large areas by spin-coating and baked at low temperatures (<170 °C) [25].

Comparison of the electrical properties of ZnO nanowire FETs with and without PMMA coating was investigated by measuring source–drain current–voltage characteristics as a function of gate voltage by using a semiconductor parameter analyzer (HP4155C). The gate voltage was applied through the highly doped silicon back gate.

3. Results and discussion

Fig. 1(a) shows the SEM image (tilted view) of ZnO nanowires vertically and uniformly grown on the entire sapphire substrate. As shown in Fig. 1(b), the PL spectrum of ZnO nanowires shows that the single near-band emission (NBE) peak at approximately 378.5 nm. This peak is attributed to the recombination of free excitons through an exciton–exciton collision process because of the 3.3 eV (376 nm) direct bandgap transition of ZnO nanowires at room temperature [26]. Although deep level emissions (broad green–yellow bands) are weak, they can be seen in the logarithmic scale PL spectrum (inset of Fig. 1(b)). Further structural characterization of the ZnO nanowires was performed by HRTEM. Fig. 1(c) and (d) shows the lattice fringes and the corresponding fast Fourier transform pattern of ZnO nanowires, respectively. These results – along with extensive bright field imaging and electron diffraction studies (not shown) – confirm that the ZnO nanowires are single crystalline with a preferred growth direction of [0 0 0 1].

Fig. 2 shows the schematic structure and FESEM image of the ZnO nanowire FETs with the back-gate configuration. Fig. 3(a) and (b) presents the transfer characteristics of the ZnO nanowire FETs with and without PMMA surface passivation for the same device. Fig. 3(c) shows the logarithmic plot of the source–drain current versus gate voltage ($I_{DS} - V_G$) curves at different source–drain biases, $V_{DS} = 0.02$, 0.05, and 0.1 V for another device.

As shown in Fig. 3, the ZnO nanowire FETs both with and without passivation exhibit the typical n-type semiconducting behaviors, since the current increases with increasing positive

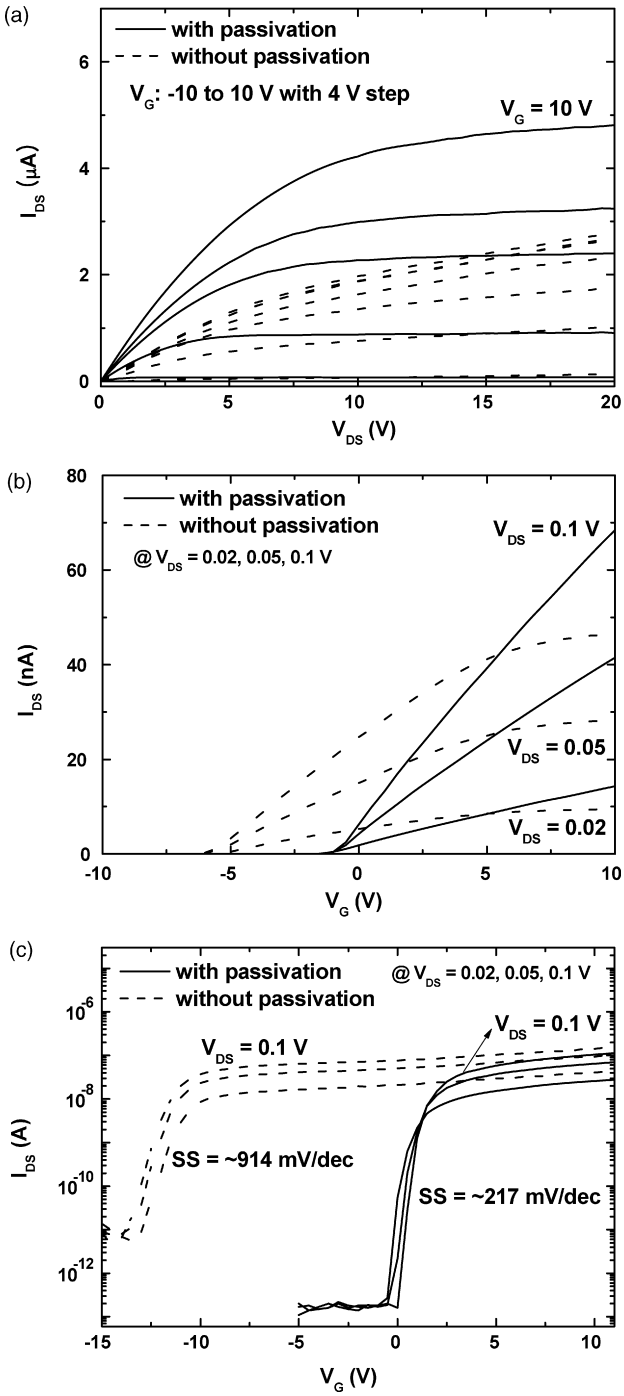

Fig. 3. (a) Source–drain current vs. voltage ($I_{DS} - V_{DS}$) characteristics at different gate voltages with and without passivation, (b) source–drain current vs. gate voltage ($I_{DS} - V_G$) characteristics at different source–drain biases for the same ZnO nanowire FET, respectively. (c) Logarithmic plot of $I_{DS} - V_G$ curves at $V_{DS} = 0.02$, 0.05, and 0.1 V for another ZnO nanowire FET device.

gate voltage, whereas it decreases down to a few picoampere (pA) with increasing negative gate voltage. It is well known that undoped ZnO generally exhibits n-type conduction due to the presence of intrinsic donor-type defects induced by deviation from stoichiometry [27,28]. From the comparison of the data with and without passivation in Fig. 3(a), the unpassivated ZnO nanowire FET devices exhibit lower conductivity (without a sat-

uration regime) as compared with passivated devices. Additionally, the threshold voltage shifts to the positive gate bias direction (Fig. 3(b)) and the current on–off ratio (I_{on}/I_{off}) is higher for the passivated devices (Fig. 3(c)). Most of the unpassivated ZnO nanowire FET devices exhibited poor electrical performance, such as a reduced current on–off ratio as well as an increased subthreshhold swing ($SS = dV_G/d(\log I_{DS})$) at $V_{DS} = 0.02$, 0.05, 0.1 V, as shown in Fig. 3(c). The current–voltage characteristics of ZnO nanowire FETs without passivation have exhibited phenomena similar to devices exhibiting short channel effects, such as punch-through in the MOSFETs [29]. The poor performance for unpassivated devices can be attributed to surface effects on the depletion region; specifically the adsorption of O_2 molecules at the ZnO nanowire surface creating a new surface path for the drain current. Consequently, it is possible for the drain depletion region in ZnO nanowire FET to reach the source depletion region at a sufficiently high drain bias. It is well known that ZnO exhibits a strong chemisorption effect of environmental molecules such as oxygen and/or oxygen-containing gaseous species through the ZnO surface [15–19]. In our study, most of the ZnO nanowire FETs with surface passivation showed good performance, due to the suppression of chemisorption by the PMMA passivation layer.

We have further estimated the transport parameters of ZnO nanowire FETs such as carrier mobility, carrier concentration, and threshold voltage. The carrier concentration is estimated from the total charge, $Q_{tot} = C_g|V_G - V_{th}|$ in the nanowire, where C_g is the gate capacitance and V_{th} is the threshold voltage required to deplete the nanowire. The gate capacitance C_g can be estimated using a model of cylinder on an infinite metal plate [30,31].

$$\frac{C_g}{L} = \frac{2\pi\varepsilon_{SiO_2}\varepsilon_0}{\cosh^{-1}(1 + h/r)} \quad (1)$$

where r is the nanowire radius, L the nanowire channel length, h the SiO_2 thickness ($h = 100$ nm), and ε_{SiO_2} is the SiO_2 dielectric constant ($\varepsilon_{SiO_2} = 3.9$). The carrier concentration at $V_G = 4$ V, $n_e = Q_{tot}/e\pi r^2 L$, was found to be in the range of 10^{16} to 10^{18} cm^{-3}. The carrier mobility in the low field region can then be calculated by

$$\mu_e = \frac{dI_{DS}}{dV_G}\frac{L^2}{V_{DS}C_g} \quad (2)$$

Through these calculations, we obtained $\mu_e = 40$–150 cm^2/V s for passivated FET devices and 5–100 cm^2/V s for unpassivated devices. For the most of ZnO nanowire FETs with passivation, the carrier mobility was improved in comparison with unpassivated devices. Furthermore, the threshold voltages were in the range from −12.5 to 2.5 V for the passivated devices and from −27.5 to −2.5 V for the unpassivated devices (Fig. 4).

Fig. 4(a) and (b) shows the distribution of the carrier mobility and threshold voltage as function of carrier concentration of ZnO nanowire FETs, respectively. Fig. 4(c) and (d) is the histogram of carrier mobility and threshold voltage of the devices with and without passivation. In Fig. 4, we plotted the results of the electrical properties of 30 passivated devices and 30 unpassivated devices for statistical comparison. It is clear that passivated devices have higher mobility and less threshold voltage than unpassivated devices. The above results (Figs. 3 and 4) show clearly that the performance of ZnO nanowire FETs is enhanced by the surface passivation with PMMA layer. The passivated ZnO nanowire FETs exhibit a clear saturation region and significant improvement in the subthreshold swing, on–off ratio (10^4 to 10^5), and mobility, which are consistent with the previously reported values for ZnO nanowire FETs [22]. Chang et al. [22] argued that the origin of the superior FET performance is attributed to the passivation of surface defect states acting

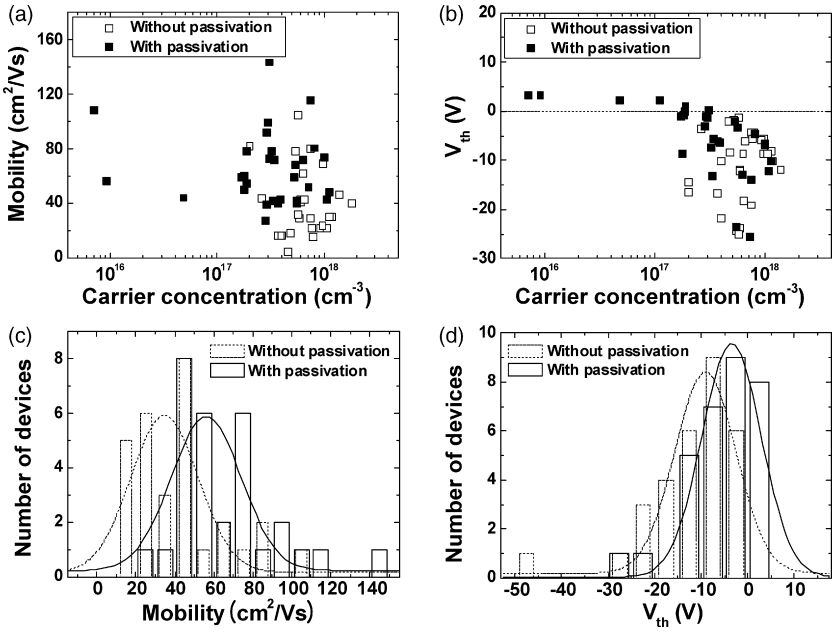

Fig. 4. (a) Mobility vs. carrier concentration and (b) threshold voltage (V_{th}) vs. carrier concentration for all ZnO nanowire FETs fabricated. Histogram of threshold voltages (a) and mobility (b) for the ZnO nanowire FETs with and without passivation.

as scattering and trapping centers and the reduction of surface chemisorption processes at oxygen vacancy sites.

4. Conclusion

In summary, we have investigated the changes in the electrical properties of ZnO nanowire FETs with and without surface passivation with organic material, PMMA. Since the ZnO nanowire FETs are strongly affected by oxygen molecules in ambient, the surface passivation on the ZnO nanowire FETs influences the electrical properties of the ZnO nanowire FETs. We observed that passivated ZnO nanowire FETs exhibited better transistor performance than the unpassivated devices.

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