Channel-length and gate-bias dependence of contact resistance and mobility for In_2O_3 nanowire field effect transistors

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We demonstrate the scaling properties of the gate-bias-dependent transfer characteristics of In_2O_3 nanowire field effect transistors (FETs) studied using a conducting atomic force microscope. The contact resistance was extracted from the scaling of the resistance of an In_2O_3 nanowire FET with respect to its channel length. This contact resistance was found to be significant for short channel devices and decreased as the gate bias increased. We also investigated the apparent and intrinsic mobilities of the nanowire FET as a function of channel length and gate bias. It was determined that the intrinsic mobility could be corrected by considering the non-negligible contact resistance. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2799960]

I. INTRODUCTION

One-dimensional nanowires have the potential to be attractive fundamental materials for use in science and technology due to their unique electrical, optical, and chemical properties.[1–4] Of these, In_2O_3 nanowires are being actively investigated as the base materials for building electronic devices such as nanowire field effect transistors (FETs) and chemical sensors.[5,6] In order to continue the miniaturization of electronic devices, the effects of scaling behaviors, such as decreasing the channel length, should be understood prior to the application of In_2O_3 nanowires in highly integrated nanowire electronics. However, the scaling properties of nanowire FETs have yet to be thoroughly investigated, as compared with the amount of research on the properties of conventional metal oxide semiconductor FETs (MOSFETs), Schottky barrier MOSFETs, or organic thin-film transistors (TFTs).[7–9] Recently, we have reported on some of the short-channel effects on In_2O_3 nanowire FETs.[10] Particularly, it has been found that as the channel length of In_2O_3 nanowire FET decreases, the threshold voltage shifts toward the negative gate-bias direction, the source-drain current and transconductance increase, and mobility decreases.[10]

In this study, we have focused on understanding the scaling properties of the gate-bias-dependent transfer characteristics of In_2O_3 nanowire FETs. Here, the channel length was varied from a controlled contact position on an In_2O_3 nanowire, using a conducting atomic force microscopy (CAFM) tip as a movable drain electrode. The contact resistances of In_2O_3 nanowire FETs were extracted by scaling the measured resistances for various channel lengths at different gate biases. Our results show that the contact resistance decreases when the gate bias increases in positive voltage. The gate-bias dependence of contact resistance has been previously reported for organic TFTs,[11–13] and the decrease in contact resistance at high gate biases has been attributed to the smaller voltage drop over the contact region via the higher charge density of the conducting channel.[14–16] Also, it has been found that transistor performance is greatly influenced by parasitic non-negligible contact resistance.[13–15] Similarly, in our study the contact resistance significantly influenced the transfer characteristics of In_2O_3 nanowire FETs with short channel lengths. In addition, we further investigated the channel-length and gate-bias dependencies of mobility for In_2O_3 nanowire FETs. Particularly, we distinguished between apparent and intrinsic mobilities, where the latter was corrected for contact resistance as a function of channel length and gate bias.

II. EXPERIMENT

A. In_2O_3 nanowire synthesis

The In_2O_3 nanowires used in this study were synthesized by carbothermal reduction followed by the catalyst-mediated heteroepitaxial growth technique.[17,18] First, a mixture of In_2O_3 powder (99.995% purity) and graphite powder (99% purity) in a 4:1 weight ratio was placed into a quartz boat, and a SiO_2/Si substrate coated with a 2 nm thin film of Au as a catalyst was placed on top of the powder. Then, the whole setup was inserted into the center of a quartz tube reactor. For nanowire growth, the reactor temperature was set between 900 and 1000 °C, while UHP-grade Ar mixed with 5% O_2 (99.999% purity) flowed at a rate of 50–100 sccm for ~35 min. After cooling, the structural properties of the single-crystalline In_2O_3 nanowires were characterized using a variety of analytic tools such as scanning electron microscopy, transmission electron microscopy, electron diffraction, x-ray diffraction, and x-ray photoelectron spectroscopy. Note that a detailed description of the structural properties of In_2O_3 nanowires has been published elsewhere.[10]

B. Electrical characterization method

In order to characterize the electrical properties of an individual In_2O_3 nanowire, In_2O_3 FETs were fabricated using optical lithography. Here, a metal electrode consisting of Ti

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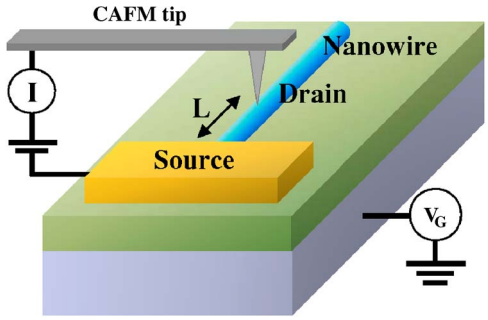

FIG. 1. (Color online) Schematic diagram of the CAFM setup for characterizing an In_2O_3 nanowire FET.

(30 nm)/Au (50 nm) layers was deposited on top of an In_2O_3 nanowire using an electron beam evaporator, followed by a lift-off process. A highly doped silicon substrate with an oxide thickness of 100 nm was used as a common back-gate electrode to modulate the carrier density in the nanowire. To take advantage of the CAFM properties, a Pt-coated tip was used as a movable drain electrode when it was in physical contact with the nanowire, as schematically illustrated in Fig. 1.[19,20] The channel length L (the distance from the CAFM tip to the source electrode) of the In_2O_3 nanowire FET was varied from 1 μm to 20 nm by placing the Pt-coated CAFM tip at specific positions on the nanowire. The radius of the CAFM probe tip was determined as ~35 nm from field emission scanning electron microscope (FESEM) images (not shown here). However, this does not mean that the size of the AFM tip contact is also 35 nm. According to the Johnson-Kendall-Roberts (JKR) elastic mechanical contact model,[21] the radius a of the junction area under the AFM tip contact can be estimated as

$$a^3 = (R/K)P_n = (R/K)\{P + 3\Gamma\pi R + [6\Gamma\pi RP + (3\Gamma\pi R)^2]^{1/2}\}, \quad (1)$$

where R is the radius of the CAFM tip end, and $K = (4/3)[(1-\nu_1^2)/E_1 + (1-\nu_2^2)/E_2]^{-1}$ where E_1, ν_1, and E_2, ν_2, are Young's modulus and Poisson's ratio of the sample (In_2O_3 in our case) and the Pt-coated tip, respectively. Using $E_1 \approx 116$ GPa, $E_2 \approx 140$ GPa, $\nu_1 \approx 0.35$, $\nu_2 \approx 0.38$,[22,23] K can be calculated to be ~97.5 GPa. P_n is the net force, which is the sum of the applied loading force P and terms due to the adhesion force. $\Gamma = 2P_c/3\pi R$ is the adhesion energy per unit area related to the adhesion force P_c which can be obtained from a force-distance characterization. As shown in Fig. 2, we obtained typical force-distance curves from which the adhesion force (P_c) between tip and In_2O_3 nanowire was determined to be 29.1 nN. Then, using Eq. (1), the radius of the contact junction area was estimated to be ~4.3 nm for the applied force of 60 nN that was the measurement condition in our experiments. Consequently, the error range of each channel length of the In_2O_3 nanowire FET is ~4.3 nm, the radius of the junction area under the AFM tip contact.

When the Pt-coated CAFM tip made physical contact with the nanowire, a drain bias V_{DS} was applied to the CAFM tip relative to the source electrode. The resulting source-drain current I_{DS} was measured in an ambient atmosphere at room temperature by a current amplifier attached to the CAFM tip. The In_2O_3 nanowire used in this study had a diameter of ~25 nm, and the electrical characteristics of the In_2O_3 nanowire FET were measured using a semiconductor parameter analyzer (HP 4145 C) at room temperature.

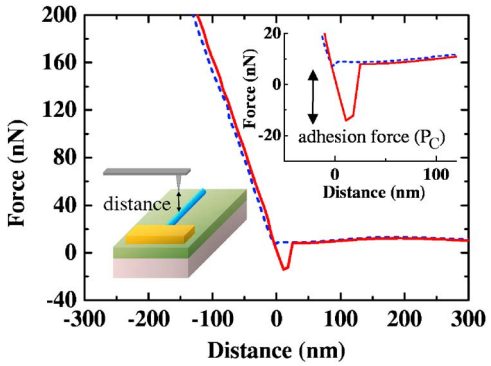

FIG. 2. (Color online) Force-distance curves measured on In_2O_3 nanowire while AFM tip is approaching the nanowire (dashed) and retracting away from the nanowire (solid). Inset is a zoomed-in region to show adhesion force (P_c) between the tip and the nanowire (~29.1 nN).

III. RESULTS AND DISCUSSION

A. Device structure and energy band diagram

The electrical configuration of the In_2O_3 nanowire FET device structure in this study can be explained using energy band diagrams, as shown in Fig. 3.[24–26] It is known that the Pt (CAFM tip) contact on the drain side of In_2O_3 nanowire forms a Schottky barrier, whereas the Ti contact on the source side is an ohmic contact.[10,27] In Fig. 3, E_{FS} and E_{FD} are the Fermi levels of the source and electrode, respectively, and Φ_{SB} is the Schottky barrier height on the drain side. The built-in potential ($eV_{bi} = \Phi_{SB} - \Phi_n$) varies depending on the forward drain voltage (V_{DS}), where e is the electronic charge and Φ_n is the potential difference between the bottom of the conduction band and the Fermi level in an n-type In_2O_3 nanowire. With the forward drain bias (positive drain bias), the injected electrons from the ohmic contact at the source electrode flow to drain electrode via either the thermionic current over the Schottky barrier, or the tunneling current through the thin barrier.

The linear shape of the $I_{DS}-V_{DS}$ curves at low drain bias [Fig. 5(a)] illustrates the ohmic behavior of an In_2O_3 nanowire FET. This ohmic behavior results from a high electric

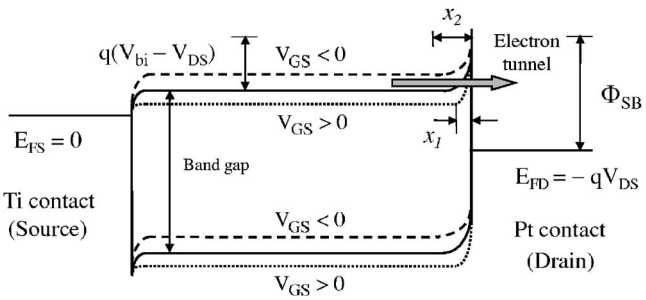

FIG. 3. Band diagram for an In_2O_3 nanowire FET for zero (solid), positive (dotted), and negative (dashed) gate biases. A forward (positive) bias is applied to the drain electrode relative to the source electrode.

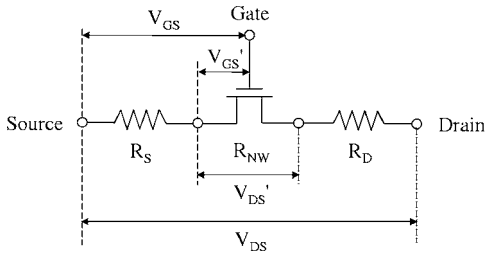

FIG. 4. An equivalent circuit model for an In_2O_3 nanowire FET showing the source and drain contact resistances.

field induced at the small contact area of the sharp CAFM tip.[10,28] When a high electric field under the CAFM tip is induced on top of the In_2O_3 nanowire surface, the Schottky barrier width at the drain side can be narrowed, and as a result ohmic contact behavior can occur.[28] As shown in Fig. 3, the change in gate voltage (V_{GS}) produces variation in the electrostatic potential, thereby changing the carrier concentration and conductance of the nanowire. When a positive V_{GS} is applied, the energy bands are lowered, meaning that electrons have accumulated in the *n*-type In_2O_3 nanowire, resulting in an increase in the conductivity. In addition, the width of the Schottky barrier (x_1) on the drain side is narrowed by the accumulated electrons, thus reducing the voltage drop across the Schottky barrier when V_{SD} is applied and contact resistance is decreased. Conversely, a negative V_{GS} will reduce the conductivity and increase the contact resistance of *n*-type In_2O_3 nanowires due to the relatively larger Schottky barrier width (x_2).[14,16]

B. Contact resistance and equivalent circuit model

A nanowire FET can be considered as a nanowire channel resistor (R_{NW}) in series with the source and drain resistors (R_S and R_D) connected to the source and drain terminals, respectively, as modeled in Fig. 4.[29] Here, the sum of R_S and R_D is the contact resistance (R_C) of the nanowire FET, and the total resistance (R_{tot}) is the sum of R_{NW} and R_C. For a small V_{DS} (linear regime), R_{tot} of the nanowire FET is given by

$$R_{tot}(L) = \frac{\partial V_{DS}}{\partial I_{DS}} = R_{NW}(L) + R_S + R_D. \tag{2}$$

The drain current in the linear regime can then be expressed as[30]

$$I_{DS} = \frac{\mu_a C}{L^2} V_{DS}(V_{GS} - V_T), \tag{3}$$

where the apparent mobility (μ_a) in a linear regime is extracted from the relationship[30,31]

$$\mu_a = \frac{1}{C}\frac{\partial I_{DS}}{\partial V_{GS}}\frac{L^2}{V_{DS}}. \tag{4}$$

Here, L is the nanowire channel length and $C = 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$ is the approximate nanowire capacitance, where ε is the dielectric constant of SiO_2 (3.9), h is the thickness of the SiO_2 layer (100 nm), and r is the radius of the In_2O_3 nanowire (12.5 nm).[32] Note that V_T is the threshold voltage defined using the peak transconductance method.[33]

For long-channel FET devices, one can disregard the contact resistance, i.e., $R_{tot} \approx R_{NW}$. However, for short-channel devices the contact resistance is needed, and the effective drain voltage ($V_{DS'}$) and effective gate voltage ($V_{GS'}$) applied to the nanowire channel can be reduced as[13]

$$V_{DS'} = V_{DS} - I_D(R_S + R_D), \tag{5}$$

$$V_{GS'} = V_{GS} - I_D R_S, \tag{6}$$

where V_{DS} and V_{GS} are the overall drain and gate voltages applied to the external terminal of the nanowire FET.

For the short-channel case, the intrinsic mobility (μ_i) after the correction for non-negligible contact resistance can be described as[10,34]

$$\frac{\partial\left(\frac{\Delta R_{tot}}{\Delta L}\right)^{-1}}{\partial V_{GS}} = \frac{\mu_i C}{L}. \tag{7}$$

Thus, the nanowire channel resistance (R_{NW}) can then be expressed in terms of intrinsic mobility as[14]

$$R_{NW}(L) \approx \frac{L^2}{\mu_i C(V_{GS} - V_T)}. \tag{8}$$

C. Gate-bias-dependent characteristics

Figure 5 summarizes a series of current-voltage characteristics of In_2O_3 nanowire FETs for different channel lengths: L=1000, 500, 200, 50, and 20 nm. Figure 5(a) presents the source-drain current versus drain voltage (I_{DS}–V_{DS}) characteristics, obtained at a range of gate voltages (V_{GS}) from −2.5 to 2.5 V, with a step of 0.5 V. It can be seen that for $V_{GS} \geq V_T$, I_{DS} increases almost linearly up to the saturation region. However, even in the saturation region the drain current still gradually increases, especially for short-channel devices. This continued current increase is known as the short-channel effect due to channel-length modulation,[10] and the current increase can be parameterized with a channel-length modulation factor (λ). When the current is extrapolated backward from the saturation region, it will meet the V_{DS} axis (I_{DS}=0) at V_{DS}=−1/λ.[29] In our nanowire FET, the λ values were determined to be 0.0346, 0.0455, 0.0667, 0.0909, and 0.1064 V^{-1} for L values of 1000, 500, 200, 50, and 20 nm, respectively. A smaller λ implies less short-channel effect. For an ideal FET device, λ is zero and the current does not increase with an increase in drain voltage (V_{DS}) after saturation. Here, the λ (=0.09 V^{-1}) for a 50 nm channel-length In_2O_3 nanowire FET is relatively small as compared to the reported value for short-channel (~50 nm) *n*-type Schottky barrier MOSFETs (λ ~0.6 V^{-1}).[8] The channel-length modulation effect in our nanowire FET could be suppressed due to small channel-length variation at high electric fields, as the small contact area of the sharp CAFM tip on the drain side and higher doping concentration (~4.8×10^{18} cm^{-3}) of In_2O_3 nanowire FET lead to a narrowing of the Schottky barrier width.[35–37]

Figure 5(b) shows the source-drain current versus gate voltage (I_{DS}–V_{GS}) at drain voltages from 0.1 to 0.5 V, with a

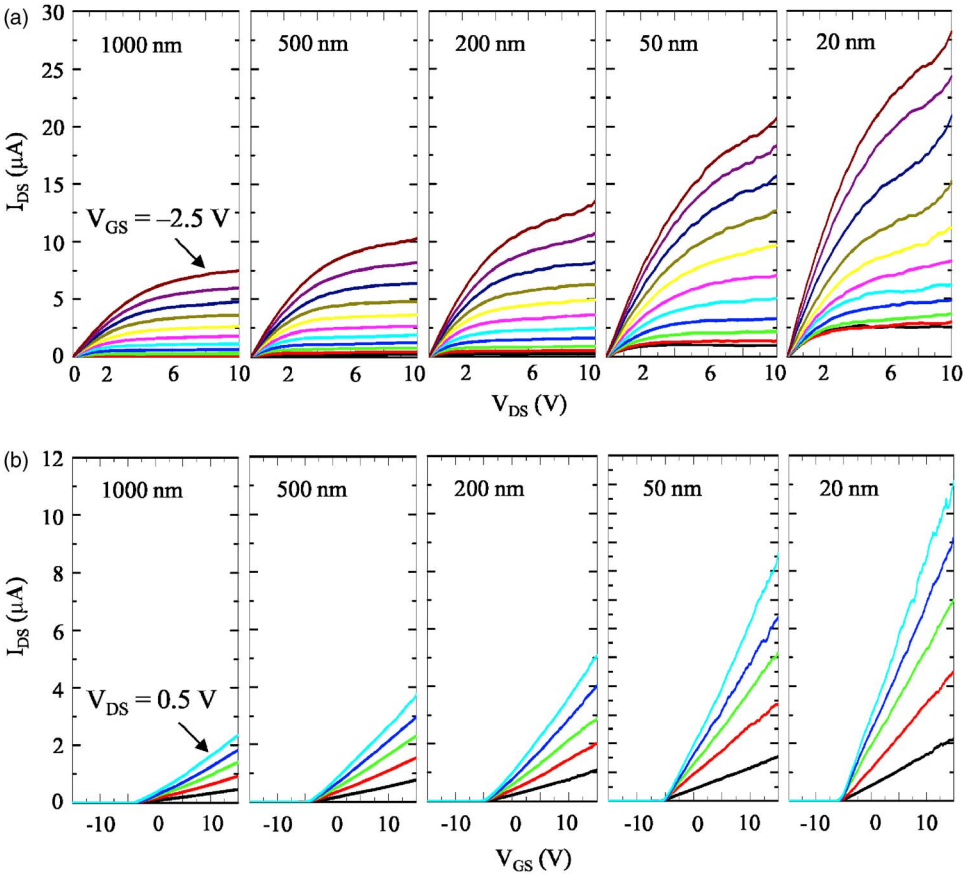

FIG. 5. (Color online) (a) $I_{DS}-V_{DS}$ characteristics for different gate biases from −2.5 to 2.5 V with a 0.5 V step, and (b) $I_{DS}-V_{GS}$ characteristics for different drain biases from 0.1 to 0.5 V with a 0.1 V step, for different nanowire channel lengths (1000, 500, 200, 50, and 20 nm, from left to right).

step of 0.1 V. The $I_{DS}-V_{GS}$ curves illustrate that the drain current I_{DS} linearly increases with an increasingly positive gate bias V_{GS} beyond the threshold voltage V_T, indicating that the device is an *n*-type depletion-mode FET. In addition, the threshold voltage was observed to shift to the negative gate bias as the channel length decreased; this threshold voltage shift phenomenon of In_2O_3 nanowires FETs has been reported elsewhere.[10]

The total resistance (R_{tot}) can be obtained from the linear regime of $I_{DS}-V_{DS}$ characteristics and plotted as a function of channel length L for different gate voltages (V_{GS}=−2.5 to 2.5 V, with a 0.5 V step), as shown in Fig. 6. In the linear operating regime of FET, it can be seen that the resistance

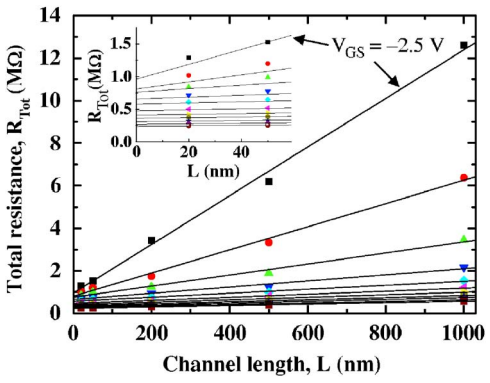

FIG. 6. (Color online) Total resistance plotted as a function of channel length for different gate biases from −2.5 to 2.5 V with a 0.5 V step. The contact resistances are obtained from the extrapolation to a zero channel length at each gate bias (inset).

varies linearly with the channel length, where the slope is proportional to the channel resistance (R_{NW}). The contact resistance (R_c) can then be extracted by extrapolating the lines to zero channel length. Thus, R_{tot} can be expressed as Eq. (2) with R_{NW} linearly dependent on the channel length L, as shown in Eq. (8) (note that the capacitance has L-dependence).

When the contact resistances obtained from the extrapolation (inset of Fig. 6) are plotted as a function of gate bias V_{GS} in Fig. 7(a), we can clearly see that the contact resistance decreases as the gate bias increases. This decrease in contact resistance can be correlated with the small voltage drop over the contact region based on the higher charge density in the conducting channel at high gate biases.[14,16] As explained earlier, the width of the Schottky barrier on the drain side is narrowed by the accumulation of electrons at higher gate biases, thereby reducing the tunneling distance, leading to more tunneling current through the narrower Schottky barrier from the channel region to the drain electrode. For this reason, when the channel is narrowed by the charge accumulating in the nanowire through the field effect imparted by the application of a higher gate bias, the parasitic contact resistance is summarily decreased.[12,14,16,38–40]

Figure 7(b) shows the channel resistances as a function of the gate bias for different channel lengths of In_2O_3 nanowire FETs. Here, both contact and channel resistances decreased as the gate voltage was increased from −2.5 to 2.5 V. It was found that the channel resistance depends more sensitively on the gate bias than the contact resistance. From the resistance data in Figs. 7(a) and 7(b), the contact resistances

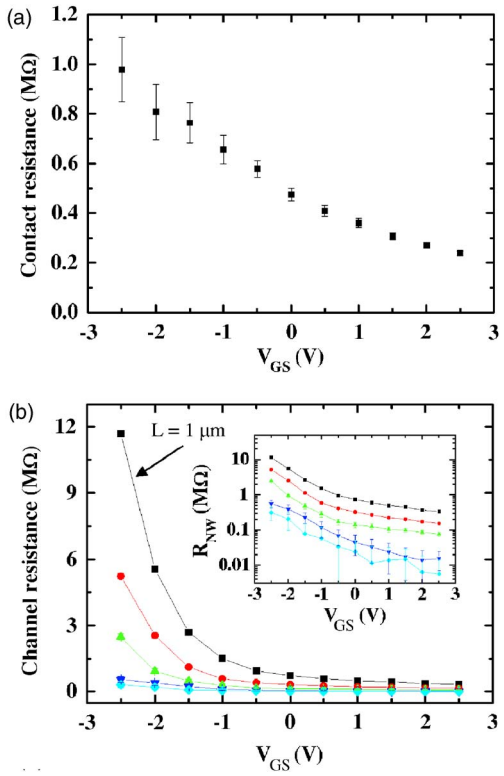

FIG. 7. (Color online) (a) Contact resistance vs gate bias, and (b) channel resistance vs gate bias for different channel lengths. Inset shows the semilog plot of the channel resistance R_{NW} vs V_{GS}.

were observed to be higher than the channel resistance for the short-channel lengths of 20 and 50 nm, which indicates that the In_2O_3 nanowire FET displayed a contact-limited performance, i.e., the transfer characteristics are limited by charge injection rather than the channel resistance itself.[13] Conversely, in the long channel-length FET of $L=1000$ nm, the channel resistance was dominant at all V_{GS}, indicating that the device performance is not contact limited. In the cases of $L=200$ and 500 nm, the channel resistance was dominant at low gate bias, whereas the contact resistance was dominant at high gate bias, indicating that the nanowire FETs of $L=200$ and 500 nm were contact limited only at a high gate-bias regime when the potential drop across the contacts was higher than that across the channel itself.[13,15]

In order to investigate the effects of contact resistance for short-channel nanowire FET devices, the current-voltage characteristics were analyzed based on the gate-bias dependence of the length-normalized drain current, i.e., by comparing the drain current multiplied by the channel length for different gate biases.[34] The length-normalized drain current for the In_2O_3 nanowire FET with $L=50$ nm channel was found to be smaller than that of the $L=200$ nm channel device, as shown in Fig. 8. The similar decrease in the length-normalized current was observed for all other shorter channel lengths (not shown here), indicating that the current in short-channel devices is primarily dominated by parasitic contact resistance.[34]

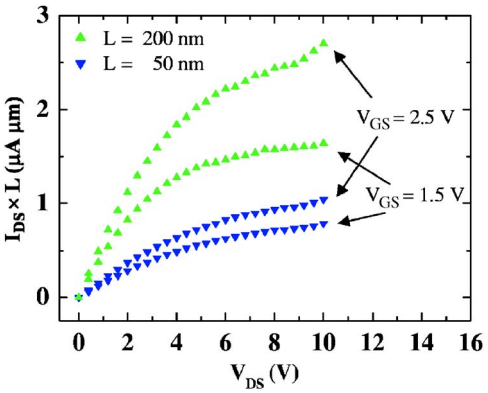

FIG. 8. (Color online) Normalized drain current vs drain voltage for an In_2O_3 nanowire FET with channel lengths L of 200 and 50 nm and gate biases V_{GS} of 1.5 and 2.5 V.

Furthermore, the significant contact resistance influences the estimation of the transistor mobility. As explained previously, the apparent mobility can be obtained as a function of the gate bias using Eq. (4). To this extent, Fig. 9(a) shows the gate-bias dependence of the apparent mobility of In_2O_3 nanowire FETs. The apparent mobility increases as the gate bias is increased. It is well known that the mobility in most transistor devices is dependent on the gate bias.[11,29,41,42] Typically, the mobility of conventional MOSFETs tends to increase linearly, saturate, and then eventually decrease with respect to the gate bias.[29,43]

The decrease at higher gate biases can be explained by the enhanced surface roughness scattering in the strong inversion layer in conventional MOSFETs.[43] However, in our experiment, we did not observe the decrease in mobility at higher gate biases, due to the relatively reduced density of states for scattering in the low dimensional channel, as compared to planar MOSFETs.[44]

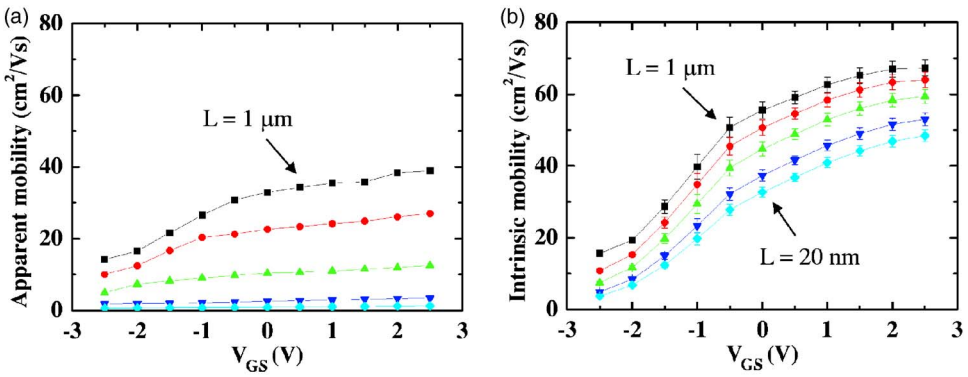

FIG. 9. (Color online) Apparent mobility (a) and intrinsic mobility (b) vs gate bias with different channel lengths ($L=1000$, 500, 200, 50, and 20 nm). The intrinsic mobility values were obtained after correcting for parasitic contact resistance.

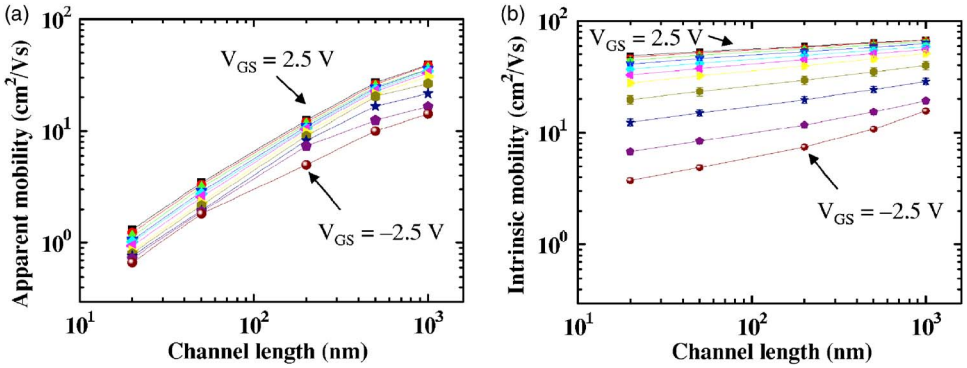

FIG. 10. (Color online) Log-log plots for apparent mobility (a) and intrinsic mobility (b) vs channel length for different gate biases (V_{GS}=−2.5 to 2.5 V with a 0.5 V step).

From Fig. 9(a), it can also be seen that the apparent mobility decreased with decreases in the channel length. This implies that a relatively large fraction of the applied source-drain voltage drops due to the contact resistance in the shorter channel FET, as compared to the longer channel FET.[34] Therefore, the contact resistance should be considered in the estimation of intrinsic mobility using Eq. (7), in which only the channel itself currently contributes.[14,34] The gate-bias dependence of intrinsic mobility is shown in Fig. 9(b), where it can be seen that the intrinsic mobility is higher than the apparent mobility in the full range of gate biases measured. We also note that the intrinsic mobility still depends on the gate bias, suggesting that the channel resistance does not linearly correspond to the gate bias, as shown in Fig. 7(b).

Figures 10(a) and 10(b) present the scaling behaviors of the apparent and intrinsic mobilities for In_2O_3 nanowire FETs. From the figures, the linear fits of the apparent and intrinsic motilities with respect to channel length in the log-log plot exhibit the dependencies of $L^{0.878}$ and $L^{0.084}$, respectively, for V_{GS}=2.5 V. It is clearly shown that the apparent mobility decreases more rapidly with a decrease in channel length as compared to the intrinsic mobility, again due to the existence of significant contact resistance in shorter channel devices.

IV. CONCLUSIONS

In conclusion, we investigated the scaling properties of an In_2O_3 nanowire FET with various channel lengths using a CAFM tip as a movable drain electrode on the nanowire. In our study, the parasitic contact resistance was extracted from the function of resistance versus channel length, and was found to decrease as the gate bias increased due to a small voltage drop over the contact region by the accumulation charge in the conducting channel at higher gate biases. We also investigated the channel length and gate-bias dependencies of the apparent and intrinsic mobilities, where the intrinsic mobility was corrected for the non-negligible contact resistance. This understanding of the scaling properties of nanowire FETs will be useful in future highly integrated nanowire-based nanoelectronic applications.

ACKNOWLEDGMENTS

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