Realization of highly reproducible ZnO nanowire field effect transistors with *n*-channel depletion and enhancement modes

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The authors demonstrate the highly reproducible fabrication of *n*-channel depletion-mode (*D*-mode) and enhancement-mode (*E*-mode) field effect transistors (FETs) created from ZnO nanowires (NWs). ZnO NWs were grown by the vapor transport method on two different types of substrates. It was determined that the FETs created from ZnO NWs grown on an Au-coated sapphire substrate exhibited an *n*-channel *D* mode, whereas the FETs of ZnO NWs grown on an Au-catalyst-free ZnO film exhibited an *n*-channel *E* mode. This controlled fabrication of the two operation modes of ZnO NW-FETs is important for the wide application of NW-FETs in logic circuits. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2748096]

One-dimensional nanostructures are currently the subject of intensive research due to their potential use as building blocks for nanoelectronic applications. Because of this, single-crystalline nanostructures of semiconducting metal oxides such as ZnO, In_2O_3, and SnO_2 have been synthesized and extensively studied.[1–3] In particular, ZnO nanostructures have attracted considerable attention due to their wide band gap (~3.4 eV), large exciton binding energy (60 meV), and potential for use in such versatile applications as ultraviolet solid-state light emitters,[4] photodetectors,[5] and sensors.[6]

In recent years, field effect transistors (FETs) using ZnO nanostructures as active channels have also been extensively investigated.[6–12] Until now the transfer characteristics of most ZnO nanowire (NW)-FET devices fabricated were typically normally on-type, *n*-channel depletion mode (*D* mode),[6–13] which exhibited nonzero current at zero gate bias and negative threshold voltages. *D*-mode NW-FETs are useful for quantitative and scalable sensing applications because the signals come from the modulation of the channel rather than the contacts.[6,7,13] However, for wide applications of NW-FETs in logic circuits, both *D*-mode FETs and enhancement-mode (*E*-mode) FETs are required.[14–19] Normally off-type, *n*-channel *E*-mode FETs, which have off current status at zero gate bias and positive threshold voltages, are preferable to *n*-channel *D*-mode FETs since there is no need for the application of a gate voltage to switch off the *E*-mode FETs.[14] Most recently, Ma *et al.* reported that nano-metal-semiconductor-FETs based on a single *n*-CdS NW can be designed to work in the *E* mode.[15] When *E*-mode transistors are employed, the power dissipation is lower and circuit design is simpler in very large scale integration level circuits.[14–17] Thus, wide scale application of NW-FETs in logic circuits requires both operation modes of transistors, working both discretely and in combination.[15–19]

In this letter, we demonstrate that the operation mode of ZnO NW-FET devices can be controlled by the growth of ZnO NWs on two different types of substrates: an Au-coated sapphire substrate and an Au-catalyst-free ZnO film. We show that the FETs of ZnO NWs grown on each substrate exhibit either *n*-channel *D*-mode or *n*-channel *E*-mode transistor performance, with highly reproducible electrical characteristics. Note that although the structure of the ZnO NW-FET device is different from the conventional metal-oxide-semiconductor transistors, the operation mode of ZnO NW-FETs is distinguished as *D* mode or *E* mode in terms of the polarity of the threshold voltage.

ZnO nanowires were synthesized by the vapor transport method, as reported elsewhere.[20] The ZnO NWs were characterized using field emission scanning electron microscopy (FESEM) and high-resolution electron microscopy (HREM). The microphotoluminescence (μPL) spectra were measured using a He–Cd laser (325 nm) as an excitation source at room temperature. We fabricated and characterized a total of 45 ZnO NW-FETs: 27 FETs of ZnO NWs grown on an Au-coated sapphire substrate and 18 FETs of ZnO NWs grown on an Au-catalyst-free ZnO film. All the devices were passivated by poly(methyl methacrylate) (PMMA). A detailed description of the fabrication of ZnO NW-FET devices has been reported elsewhere.[20,21] The FET characteristics of ZnO NWs grown on both substrates were investigated using a semiconductor parameter analyzer (HP4155C).

Figures 1(a) and 1(b) show typical HREM images of ZnO NWs grown on an Au-coated sapphire substrate and on an Au-catalyst-free ZnO film, respectively. Insets of Figs. 1(a) and 1(b) are computed fast Fourier transform patterns obtained from the lattice fringes of ZnO NWs. These result patterns along with transmission electron diffraction patterns taken from the entire nanowire structure (not shown) indicate that the ZnO NWs grown on both substrates are single crystalline with a preferred growth direction of [0001]. Both the low magnification images and the HREM images allow com-

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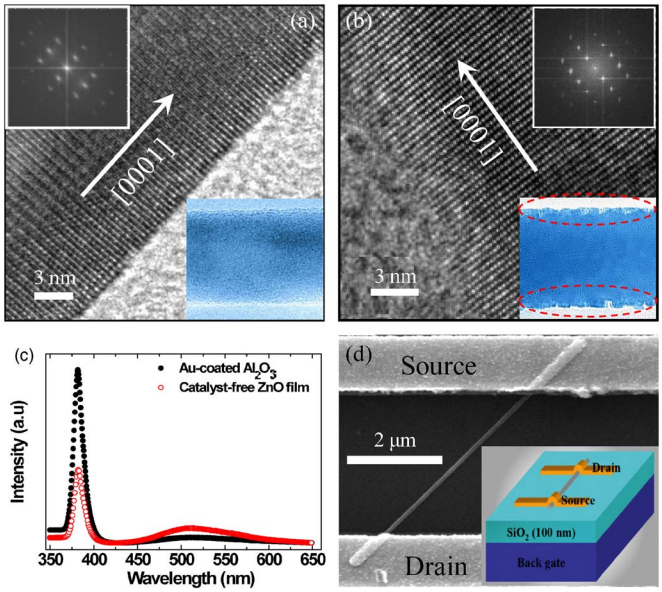

FIG. 1. (Color online) HREM images of ZnO NWs grown on (a) an Au-coated sapphire substrate and (b) an Au-catalyst-free ZnO film. Insets are computed fast Fourier transform patterns (upper) and low magnification TEM images (lower). (c) μPL emission spectra of ZnO NWs on the two substrates showing emissions at approximately 378 nm. (d) A FESEM image of a single ZnO NW connected between source and drain electrodes in FET device structures (inset).

parison between the surface structures of the ZnO NWs grown on the different types of substrates. Compared to the ZnO NWs grown on an Au-coated sapphire substrate, the ZnO NWs grown on an Au-catalyst-free ZnO film are seen to be significantly rougher across the surfaces parallel to the growth direction, as is apparent in the HREM images, and as is indicated by the circled regions in low magnification images [inset of Fig. 1(b)]. Figure 1(c) shows the μPL spectra of ZnO NWs grown on the two different substrates. Note that we measured the μPL spectra from the ZnO NWs transferred from the growth substrates to a silicon wafer in order to eliminate signals coming from the ZnO film substrate itself. The ZnO NWs grown on an Au-catalyst-free ZnO film show a stronger green emission in the PL spectrum than those grown on an Au-coated sapphire substrate. Since it is generally agreed that the green emission is a surface-related process,[22] the PL spectra suggest that the ZnO NWs grown on an Au-catalyst-free ZnO film have a significantly greater number of surface defect sites. Figure 1(d) shows the SEM image of a single ZnO NW connecting the source and drain electrodes in the FET device structure (inset).

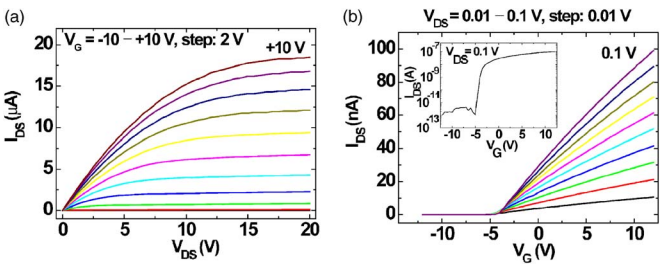

FIG. 2. (Color online) (a) Output characteristics (I_{DS}-V_{DS}) and (b) transfer characteristics (I_{DS}-V_G) for n-channel depletion-mode FET of ZnO NWs grown on an Au-coated sapphire substrate. The inset shows the semilogarithmic plot of the I_{DS}-V_G curve at V_{DS}=0.1 V.

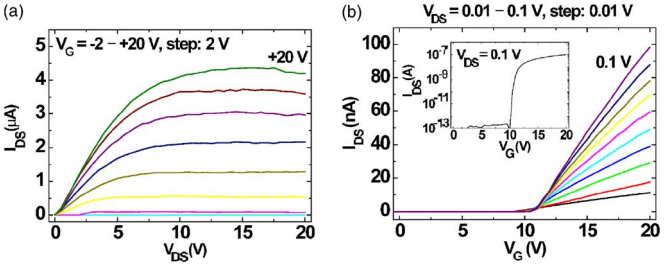

FIG. 3. (Color online) (a) Output characteristics (I_{DS}-V_{DS}) and (b) transfer characteristics (I_{DS}-V_G) for n-channel enhancement-mode FET of ZnO NWs grown on an Au-catalyst-free ZnO film. The inset shows the semilogarithmic plot of the I_{DS}-V_G curve at V_{DS}=0.1 V.

The electrical characteristics of ZnO NW-FETs are summarized in Figs. 2 and 3. Figures 2(a) and 2(b) show the representative data of source-drain current versus voltage (I_{DS}-V_{DS}) and source-drain current versus gate voltages (I_{DS}-V_G) for an n-channel D-mode FET using ZnO nanowires grown on an Au-coated sapphire substrate. The I_{DS}-V_{DS} curves [Fig. 2(a)] of an n-channel D-mode FET have well-defined linear regimes at low biases and saturation regimes at high biases. This is in good agreement with the characteristics of ZnO nanobelt FETs with Ti/Au Ohmic contacts.[14] The I_{DS}-V_G curves [Fig. 2(b)] show that the threshold voltage V_{th} is −4.14 V, indicating n-channel D-mode behavior. The I_{DS}-V_G plot in the semilogarithmic scale displays an on/off current ratio as large as 10^5 [inset of Fig. 2(b)]. In contrast, in the I_{DS}-V_G curves [Fig. 3(b)] for FETs using ZnO nanowires grown on an Au-catalyst-free ZnO film, the threshold voltage V_{th} is +10.85 V, indicating n-channel E-mode behavior. The I_{DS}-V_G plot in the semilogarithmic scale shows an on/off current ratio as large as 10^6 [inset of Fig. 3(b)].

In order to study the reproducibility of such different operation modes of ZnO NW-FETs, we examined all 45 FETs of ZnO NWs grown on two different substrates. Figure 4 summarizes the threshold voltages for all of the measured FETs. As seen in Fig. 4, all FETs created from ZnO NWs grown on an Au-coated sapphire substrate showed negative threshold voltages, indicating that more negative gate bias should be applied to deplete carriers in the channel to reduce channel conductance, since the n-channel for current flow already exists at zero gate bias. These are normally on-type, n-channel D-mode transistors.[19] In the contrast, all FETs of ZnO NWs grown on an Au-catalyst-free ZnO film showed

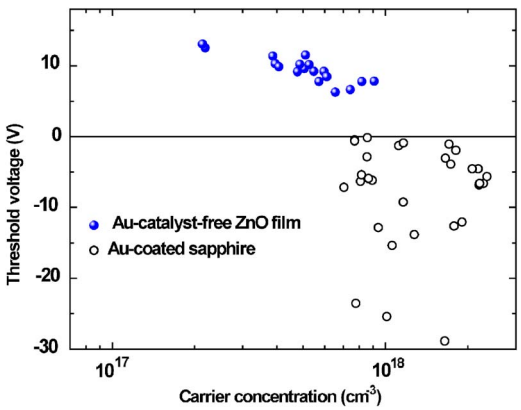

FIG. 4. (Color online) Threshold voltage (V_{th}) vs carrier concentration (at V_G=15 V) for all the fabricated ZnO NW-FET devices.

positive threshold voltages, indicating that more positive gate bias is needed to make the channel, since the channel current does not flow at zero gate bias. These are normally off-type, *n*-channel *E*-mode transistors.[19]

The threshold voltages can be used to estimate the carrier concentration from the total charge, $Q_{\mathrm{tot}}=C_{\mathrm{G}}|V_{\mathrm{G}}-V_{\mathrm{th}}|$ in the nanowire, where C_{G} is the gate capacitance and V_{th} is the threshold voltage required to deplete the NW.[20] The gate capacitance C_{G} can be estimated using a model of a cylinder on an infinite metal plate,[20,23]

$$\frac{C_G}{L}=\frac{2\pi\varepsilon_{\mathrm{SiO_2}}\varepsilon_0}{\cosh^{-1}((r+h)/r)}, \tag{1}$$

where r is the NW radius (110 ± 20 nm), L is the NW channel length, h is the SiO_2 thickness ($h=100$ nm), ε_0 is the permittivity of free space, and $\varepsilon_{\mathrm{SiO_2}}$ is the dielectric constant of SiO_2 (3.9). Thus, the carrier concentration, $n_e=Q_{\mathrm{tot}}/e\pi r^2L$, can be determined at a gate bias of 15 V, for all the individual ZnO nanowire FET devices, as plotted in Fig. 4.

Most ZnO NW-FETs with Ti/Au Ohmic contacts reported to date have exhibited *n*-channel *D*-mode behavior.[8,10,11] However, in our study, both operation modes were observed. Although the mechanism of different operation modes of FETs of the ZnO NWs grown on two different types of substrates is as of yet not clear, one possible origin of the different operation modes may be related to surface defect states, which act as scattering and trapping centers. Hossain *et al.* reported that ZnO thin film transistors (TFTs) without grain boundaries exhibited *D*-mode characteristics, whereas ZnO TFTs with grain boundaries exhibited *E*-mode behavior due to the presence of the trap sites.[24] Dehuff *et al.* also showed that TFTs with zinc indium oxide channel layers exhibited clear *D*-mode and *E*-mode behavior for devices processed at 600 and 300 °C, respectively.[25] They reported that the *E*-mode device behavior is attributed to deep traps in the channel or at the interface.

Consequently, as shown in Figs. 1(b) and 1(c), the ZnO NWs (grown on an Au-catalyst-free ZnO film) with significantly rough edge surfaces can have a high density of trap sites at their interface, such as at the passivation layer (PMMA)-ZnO interface, the ZnO–SiO_2 interface, or the ZnO–Ti/Au interface. Additionally, the ZnO–Ti/Au contacts have been reported to exhibit Ohmic behavior via thermionic field emission due to an increase in oxygen vacancies near the ZnO surface.[26] However, when a high density of surface states exists—as in the case of ZnO nanowires grown on an Au-catalyst-free ZnO film—electrons donated from the oxygen vacancies will be trapped in the interface states, prohibiting their contribution as channel carriers. Therefore, the different operation modes of ZnO NW-FETs could be attributed to difference in the density of surface defect states of ZnO NWs. However, the detailed mechanism and the dependence of the density of surface states on threshold voltage will need to be systematically investigated.

In summary, we have fabricated and characterized FETs using ZnO NWs grown by the vapor transport method on two different types of substrates. All FET devices using ZnO NWs grown on an Au-coated sapphire substrate exhibited *n*-channel *D*-mode behavior, whereas the devices using ZnO NWs grown on an Au-catalyst-free ZnO film exhibited *n*-channel *E*-mode FET behavior. Realization of highly reproducible ZnO NW-FETs with both *D* mode and *E* mode has the potential to offer a number of advantages in logic applications.

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