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Review paper

Electronic properties of metallic nanoclusters on semiconductor surfaces: Implications for nanoelectronic device applications

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Abstract

We review current research on the electronic properties of nanoscale metallic islands and clusters deposited on semiconductor substrates. Reported results for a number of nanoscale metal–semiconductor systems are summarized in terms of their fabrication and characterization. In addition to the issues faced in large-area metal–semiconductor systems, nano-systems present unique challenges in both the realization of well-controlled interfaces at the nanoscale and the ability to adequately characterize their electrical properties. Imaging by scanning tunneling microscopy as well as electrical characterization by current–voltage spectroscopy enable the study of the electrical properties of nanoclusters/semiconductor systems at the nanoscale. As an example of the low-resistance interfaces that can be realized, low-resistance nanocontacts consisting of metal nanoclusters deposited on specially designed ohmic contact structures are described. To illustrate a possible path to employing metal/semiconductor nanostructures in nanoelectronic applications, we also describe the fabrication and performance of uniform 2-D arrays of such metallic clusters on semiconductor substrates. Using self-assembly techniques involving conjugated organic tether molecules, arrays of nanoclusters have been formed in both unpatterned and patterned regions on semiconductor surfaces. Imaging and electrical characterization via scanning tunneling microscopy/spectroscopy indicate that high quality local ordering has been achieved within the arrays and that the clusters are electronically coupled to the semiconductor substrate via the low-resistance metal/semiconductor interface.

Introduction

With further downscaling of semiconductor devices, there will be a transition from the present fabrication technology at the micrometer length scale to a new technology at the nanometer length scale. Successful nanofabrication protocols will require a clear understanding of physical properties of nanometer scale systems (Nalwa, 2000).

The ability to easily fabricate nanometer scale structures is an essential ingredient for further advances in nanotechnology. Direct use of conventional lithographic techniques such as electron beam lithography (Johnson et al., 1998) or scanning probe microscope-related nanolithography (Dai et al., 1998; Hong et al., 1999) become slow when used to define nanoscale features. Recently self-assembly techniques have attracted interest for nanoscale device applications because these techniques offer the potential to fabricate nanoscale elements such as quantum dots and electronic device configurations of these nanoscale elements without direct use of conventional lithographic techniques. A number of self-assembly techniques have been reported for fabricating nanoscale structures of clusters, quantum dots, and wires (Murray et al., 1995; Andres et al., 1996b; Korgel & Fitzmaurice, 1998;

Chung et al., 1998; Brune et al., 1998; Kiely et al., 1998; Fan et al., 1999). A recurring theme in these self-assembly protocols is their use of pre-formed nanoscale metallic clusters.

In what follows, we review recent studies of nanoscale metallic clusters deposited on semiconductor substrates with a view toward future nanoelectronic applications. At present, it is difficult to predict in any great detail what ultimate electronic functionality will be gained using nanoparticles. The near future will almost certainly exploit the small size and regular geometric shape of nanoscale crystalline clusters in prototype designs of simple electronic circuits similar to those used in current practice. As discussed below, functionalities like non-linear I–V characteristics and nanoscale ohmic contact have already been demonstrated for vertical electron transport between a metal nanoparticle and a semiconductor substrate.

In the longer term, the deposition of cluster networks on active semiconductor surfaces to provide a periodic lateral modulation of the electronic properties of the underlying substrate seems promising. Patterning achieved via self-assembly of the clusters could either be transferred into the substrate via selective eching using the clusters as an etch mask or could be induced by electronic interactions at the cluster–substrate interface. The ability to functionalize a cluster network with linking molecules of choice adds a low-cost design flexibility that seems attractive. Tailoring the lateral electron transport in a cluster network, placed between two or more contact pads as well as the vertical electron transport into a semiconducting substrate can be exploited in advanced computational, biological, or chemical sensing applications. Scenarios for attaining useful electronic functionality in cluster-based 'devices' have already been proposed (Roychowdhury et al., 1996; Bandyopadhyay & Roychowdhury, 1996; Datta et al., 1998; Snow & Wohltjen, 1998; Wohltjen & Snow, 1998)

Within this context, semiconductor substrates are of particular interest because at this time they seem to provide the most direct path to useful electronic functionality. Published work falls into three general categories which include single electron tunneling (SET) devices, nanoscale Schottky barriers and nanoscale ohmic contacts. Almost all of the published work relies heavily on scanning probe microscopy. A further important issue is related to the accurate positioning of metallic clusters on semiconductors. While a variety of studies have discussed some of the recent work which offers promise in this area and have shown the potential of pushing and locating clusters with scanning probe tips, few studies have been reported which offer a global solution to the important problem of accurate cluster positioning. In what follows, we will discuss some very recent work which offers promise in this area.

We have attempted to accurately survey the literature and summarize interesting work involving metallic nanoclusters on semiconductors through 1999. We apologize in advance if any work has been inadvertently overlooked in the review that follows.

Nanocluster synthesis and deposition

Nanocluster synthesis and deposition on semiconductors follow a wide range of protocols. Studies have been reported in which submonolayer coverage of metal adatoms have been evaporated onto various substrates and allowed to coalesce into small nanometer-size islands, scanning probe tips have been pulsed to cause a deposition of small numbers of atoms in localized regions, clusters have been deposited from colloids, or by electrochemical processes. Table 1 summarizes various fabrication techniques of nanoscale metallic islands on semiconductor substrates.

Many of these techniques produce small, nanometer-size deposits that are often called 'nanoclusters', but the structure of the 'nanocluster' and the nature of its interface to the semiconductor surface is often not well defined or characterized. With this view in mind, it seems clear that the ability to fabricate well-controlled geometry (i.e. crystalline) metallic clusters is highly desirable. Metal clusters in the size range from 1 to 10 nm in diameter are known to be equiaxed and can be synthesized as well-faceted single crystals.

Aerosol synthesis of Au nanoclusters

One proven approach to the fabrication of crystalline nanoclusters of controlled size is using an aerosol reactor. For example, nanometer size single crystal Au clusters with controlled diameters (ranging from ~ 2 to ~ 20 nm) have been synthesized using an aerosol reactor known as a Multiple Expansion Cluster Source (MECS). A schematic of the MECS is shown in Figure 1.

In the MECS, bare Au clusters are nucleated, grown, and annealed in an inert gas (helium or argon) at reduced pressures. After gas phase annealing each cluster is an fcc crystal in the shape of a truncated octahedron. The bare Au clusters are encapsulated and

Table 1. Summary of studies on metallic nanoclusters on semiconductors. The size of cluster was determined from the height of cluster in STM topographic image. All the characterization was done at room temperature

Semiconductor substrate	Metallic cluster	Deposition environment	Cluster fabrication	Characterization environment	Observation	Reference
p-Si(111)	Au ∼ 3 nm	*in-situ*	Deposition from tip	UHV STM	SET	Radojkovic et al., 1996
p-Si(100)	Au ∼ 1 nm	*in-situ*	Deposition from tip	UHV STM	SET	Hu et al., 1999
p-Si(111)	Ag ∼ 0.6 nm	*ex-situ*	Thermal evaporation	UHV STM	SET	Park et al., 1999
n-GaAs(110)	Ag ∼ 1.5 nm	*in-situ*	Thermal evaporation	UHV STM	SET	Jiang et al., 1999
n-GaAs and n-InP	Pt 20–100 nm	*in-situ*	Electrochemical process	Air AFM	Schottky barrier	Hasegawa et al., 1999; Sato et al., 1999
n-Si(111)	Au >10 nm	*ex-situ*	Thermal evaporation	Air STM	Schottky barrier	Gheber et al., 1994
TiO_2	Cu 5–20 nm	*in-situ*	Thermal evaporation	UHV STM	Schottky barrier	Carroll et al., 1997
p-GaAs(110)	Fe 1–10 nm	*in-situ*	Epitaxy (MBE)	UHV STM	Schottky barrier	First et al., 1989
n-GaAs(100)	Au ∼ 4 nm	*ex-situ*	Deposition from colloid	UHV STM	Ohmic contact	Lee et al., 1999; 2000a

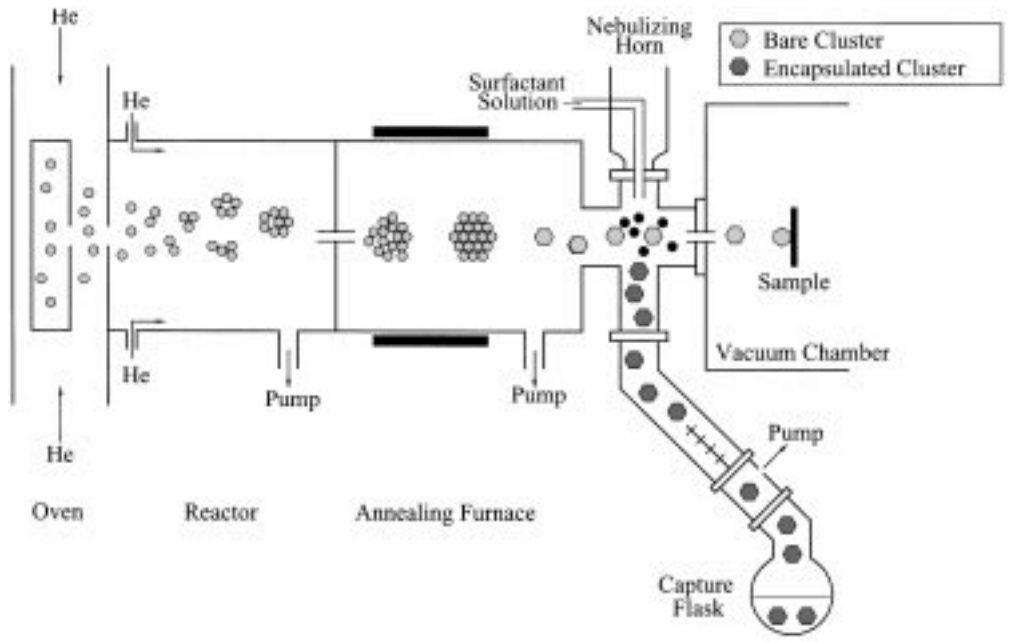

Figure 1. Schematic of the Multiple Expansion Cluster Source (MECS).

protected from agglomeration by spraying a surfactant, e.g. dodecanethiol [$CH_3(CH_2)_{11}SH$, denoted as DDT] solution into the aerosol flow downstream of the MECS. Detailed descriptions of the MECS can be found elsewhere (Bowles et al., 1981; Choi & Andres, 1987; Chao & Andres, 1994).

The DDT encapsulated Au nanoclusters are soluble and form stable colloidal solutions in many nonpolar

organic solvents, such as hexane, heptane, chloroform, mesitylene, etc. These encapsulated Au nanoclusters behave like simple chemical compounds; they can be precipitated, re-dissolved, and chromatographically separated without any apparent damage (Brust et al., 1994; Whetten et al., 1996). Compared to various liquid phase synthesis methods, this aerosol synthesis has the following advantages: (i) the clusters are synthesized and annealed at very high temperatures so that each cluster is a well-faceted fcc single crystal; (ii) the clusters are charge neutral, which eliminates potential offset charge problems; (iii) both bare and encapsulated nanoclusters can be obtained, enabling studies on the effects of encapsulation on the crystal structure and other properties of the nanoclusters; (iv) the encapsulant can be displaced by other organic molecules in order to control the structural and electronic properties of the cluster networks (Andres et al., 1996b).

Semiconductor substrates

Only a few semiconductor substrates have been chosen to support nanoclusters. These substrates include Si, native oxide (SiO_2) on Si, GaAs, and InP. Since semiconductor substrates can provide device functionality and circuitry, the electronic integration of nanoclusters with various semiconductor device structures is of particular interest.

Substrate considerations

Semiconductor substrates should be flat enough at the nanometer scale for the experimental characterization of deposited metallic nanoclusters. A rough substrate surface having average roughness comparable to the dimension of the nanoclusters will cause difficulty in distinguishing clusters from features of substrate itself.

Chemical stability of semiconductor surfaces (e.g. resistance to oxidation upon air exposure) can be an important benefit in the case when *ex-situ* processing of deposited nanoclusters is required. Semiconductor materials such as Si and GaAs are known to oxidize quickly when exposed to air, resulting in an electrical insulating layer and a non-uniform, rough surface. Cleaving substrates *in-situ* is one solution to this problem (First et al., 1989; Jiang et al., 1999). Another approach is to intentionally passivate semiconductor surfaces to prevent oxidation and non-uniformity (Lee et al., 1999).

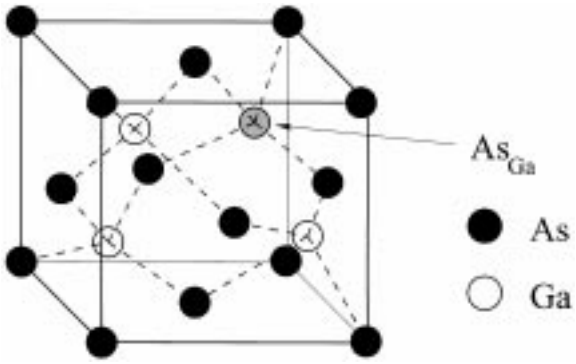

Figure 2. Model structure of LTG:GaAs showing an arsenic antisite defect (As_{Ga}).

Low temperature grown GaAs

Surface modification of semiconductor substrates can produce desirable properties for nanocluster research. For instance, a layer of low-temperature grown GaAs (LTG:GaAs) (Melloch et al., 1995) has been found to have a number of useful properties that make it a promising candidate for the study of deposited metallic nanoclusters. LTG:GaAs shows many interesting electronic properties that have been attributed to the $\sim$1–2% excess arsenic incorporated during growth. For As-grown material, the excess arsenic results in a high concentration ($\sim 1 \times 10^{20}$ cm^{-3}) of point defects, primarily as arsenic antisite defects (Melloch et al., 1995). A noteworthy consequence of these antisite defects is the introduction of a band of states located in the GaAs bandgap. These states prevent the GaAs surface from rapidly oxidizing due to the relatively low concentration of minority carrier holes in the surface layer arising from the small minority carrier lifetime in LTG:GaAs material (Hong et al., 1996; Ng et al., 1996). Therefore, LTG:GaAs material can be a proper material for nanometer scale device applications since the rapid oxidizing on Si and GaAs causes non-uniform electric contacts. Figure 2 is a model structure of LTG:GaAs indicating an arsenic antisite defect (As_{Ga}).

Experimental characterization

Any tool to successfully characterize a nanoscale system requires both a direct imaging capability coupled with a nanometer scale characterization capability. High resolution microscopic techniques, such

as scanning electron microscopy (SEM), transmission electron microscopy (TEM), scanning tunneling microscopy (STM) and atomic force microscopy (AFM) can be used to obtain direct images of the material surface at the nanometer scale. Other surface analytical techniques, such as X-ray photoemission spectroscopy (XPS), ultraviolet photoemission spectroscopy (UPS), X-ray diffraction and low-energy electron diffraction (LEED) can only provide spatially averaged information. Among these techniques, however, only STM and STM-based spectroscopic techniques can provide a proper experimental tool for both imaging and characterization.

STM was invented in early 1980's by Binnig and Rohrer and is a powerful technique to image the real space of a surface structure (Binnig et al., 1982). STM and STM-related techniques are now widely used in the areas of physics, chemistry, material science, and biology. In earlier times, the main application of STM was to image the surface of a material. Nowadays, STM and STM spectroscopic techniques enable the study of electrical properties of nanoscale elements. STM has also been used to modify the surface at the atomic scale (Eigler & Schweizer, 1990; Crommie et al., 1993). Therefore, STM has become an important technique in surface science both for characterization of the nanometer scale devices and for enabling novel nanolithographic fabrication.

Usually, a ultra high vacuum (UHV) STM is used to locate nanoclusters and probe their electronic properties. Typically, the STM head is housed in an ion-pumped chamber with a pressure less than 1×10^{-10} Torr.

Metallic nanoclusters on semiconductor substrates

The electronic properties of metallic nanoclusters on semiconductors depend on the metal comprising the cluster, the size of cluster, the semiconductor substrate, and the fabrication technique. Generally speaking, metal/semiconductor nanostructures fall into three broad categories: (i) SET devices, (ii) nanoscale Schottky barriers, and (iii) nanoscale ohmic contacts. The first category relies on conditions when the size of a cluster is reduced to a few nanometers. The second two categories rely on a confined metal/semiconductor type interface. Such interfaces could produce Schottky barriers or ohmic contacts based on the work functions and other electronic properties, such as Fermi level pinning, barrier height, and barrier width.

Single electron tunneling

When the size of a cluster on a semiconductor is a few nanometers, SET effects such as Coulomb blockade and Coulomb staircase can be observed. Similar effects were previously observed for nanoclusters on metal substrates (Dorogi et al., 1995; Andres et al., 1996a; Bigioni et al., 1999).

As summarized in Table 1, Coulomb blockade or Coulomb staircase phenomena were studied using Au clusters on p-Si(111) (Radojkovic et al., 1996; Hu et al., 1999), Ag clusters on p-Si(100) (Park et al., 1999), and Ag clusters on n-GaAs(110) (Jiang et al., 1999). The size of the cluster in these studies was determined from the cluster height in STM topographic images since the lateral size of a cluster in an STM image is significantly broadened by tip convolution effect. When the size of cluster is reduced to the nanometer scale, the capacitance of the cluster/substrate structure can be low enough so that the single electron charging energy $e^2/2C$ is large compared to the thermal energy $k_B T$ (k_B is Boltzmann's constant) which is about 26 mV at room temperature. For asymmetric structures, this effect is observed as steps in an I–V curve or oscillations in dI/dV and is known as a Coulomb staircase. Also the tunneling probability is very small for voltages smaller than $e/2C$, resulting an energy gap in this voltage region. This phenomenon is referred to as Coulomb blockade. Typically single electron tunneling effects at room temperature can be observed in a cluster less than ~ 3 nm in diameter.

Figure 3 is an example STM I–V (a) and dI/dV (b) data which show both Coulomb blockade and Coulomb staircase as SET effects through ~ 3 nm Au cluster on p-Si(111) (Radojkovic et al., 1996). The overall I–V shape in Figure 3 is asymmetric and somewhat resembles that of a Schottky contact. Since a p-type semiconductor was used, there is more current for positive bias compared with the negative bias regime (the system is forward biased by applying a positive sample voltage). The structure was modeled by a double-barrier junction with a set of two resistors and two capacitors.

Nanoscale schottky barriers

When the size of a metallic cluster on a semiconductor is not small enough for SET effects, the structure can

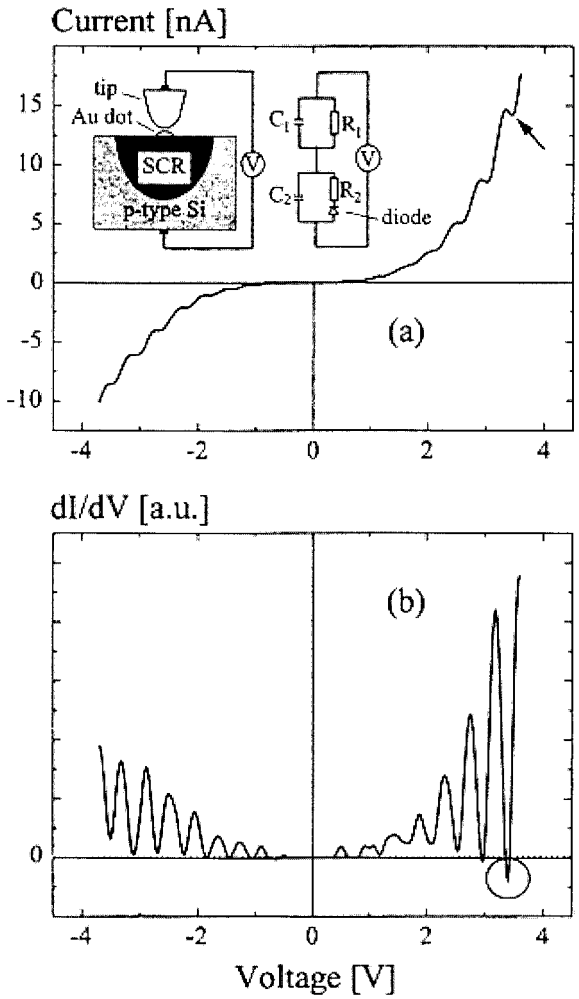

Figure 3. (a) *I–V* characteristic obtained on a Au dot, showing equidistant steps of $\simeq 430$ mV. The inset illustrates the schematic of the experimental arrangement under zero-bias conditions, comprising the equivalent circuit with the resistances and capacitances R_1, C_1 and R_2, C_2, respectively (SCR: space-charge region). (b) numerical derivation of (a) showing periodical oscillation. Arrows in (a) and circle in (b) indicate the occurrence of regions with negative differential resistance (NDR). (From Radojkovic et al., 1996.)

exhibit Schottky barrier behavior. Nanoscale Schottky barriers were fabricated with Pt clusters on n-GaAs and n-InP (Hasegawa et al., 1999; Sato et al., 1999), Au clusters on n-Si(111) (Gheber et al., 1994), and Cu clusters on TiO_2 (Carroll et al., 1997). Figure 4 is an *I–V* curve measured on a Pt cluster on n-GaAs using a conducting AFM tip (Sato et al., 1999), where the data shows typical Schottky barrier (diode) characteristic.

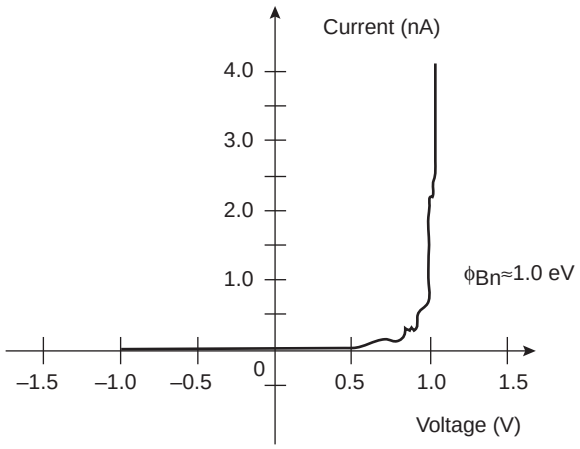

Figure 4. *I–V* curve measured at Pt dot/n-GaAs contacts. (From Sato et al., 1999.)

Many of the major issues in large-area metal/semiconductor interfaces are also of primary concern for nanoscale interfaces. For large-area Schottky (metal/semiconductor) contacts, the most fundamental issue is the control of the Schottky barrier height. The control of the Schottky barrier height by varying the contact metal indicates that interface states do not play a dominant role. The control of interface characteristics at the nanometer scale, e.g. between nanoclusters and semiconductor surfaces, would be of comparable interest.

Many studies of the interface of metal/semiconductor structures have been reported. For example, in a semiconductor such as n-GaAs, *ex-situ* techniques typically find that the Schottky barrier height does not change significantly as the metal work function is changed (Woodall & Freeouf, 1981; Tersoff, 1988). In this case, the surface Fermi level is 'pinned' at approximately midgap. There is still debate as to whether this is an intrinsic effect due to effects such as a metal-induced gap states (MIGS) (Heine, 1965; Louie & Cohen, 1976; Tersoff, 1984; Monch, 1999) or an extrinsic effect due to oxidation of the semiconductor surface before metal deposition (Woodall & Freeouf, 1981). There have been reports of unpinned surface Fermi levels, i.e. Schottky barrier heights change in proportion to the deposited metal work function for *in-situ* Schottky contacts (Brillson et al., 1988). There is also evidence that Schottky barrier heights smaller than those associated with midgap pinning have been achieved in *ex-situ* nonalloyed ohmic contact structures employing a LTG:GaAs surface layer (Chen et al., 2000).

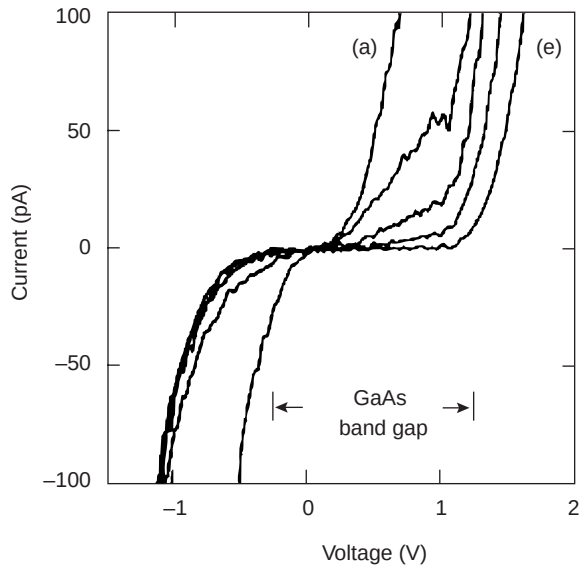

Figure 5. Tunneling current vs. tip distance from the Fe cluster. Curve (a) is on the cluster. Curve (b) to curve (e) correspond to distances from the cluster edge of 3.7, 6.7, 9.6 and 14.3 Å. (From First et al., 1989.)

The observation of MIGS in nanoscale barriers has been reported within the bandgap of a nanoscale Schottky barrier structure formed using Fe clusters on GaAs(110), as shown in Figure 5 (First et al., 1989). The metallic behavior in the I–V curve (a) was attributed as metallic cluster-induced gap states in tunneling to the GaAs substrate. When I–V was attempted far from the cluster, GaAs features [curve (e)] were observed.

One of the key difference between metal/semiconductor interfaces at the nanometer scale and at the micrometer scale is the relative influence of the semiconductor surface surrounding the metal contact. In large-area contacts, the contact characteristics (Schottky barrier height, leakage current) are typically viewed as being dominated by the area under the contact, rather than by the effects of the open surface surrounding the contact. However, in nanometer scale contacts, the ratio between the contact area and the active area of the interface region around a contact (the region over which a potential difference is dropped) can be small. In this case the characteristics of the surrounding unmetallized surface can have a significant impact on the measured Schottky barrier height.

Hasegawa et al., studied the dependence of Schottky barrier height on the metal work functions with nanoscale (20–50 nm in diameter) Schottky barriers fabricated using an *in-situ* electrochemical process (Hasegawa et al., 1999). Pt/InP Schottky barrier height was found to increase as the cluster size is reduced. This effect was attributed to an 'environmental' Fermi level pinning surrounding the cluster, i.e. the effect of the surface Fermi level in the semiconductor region surrounding the cluster. In this case, the unmetallized InP surface was pinned at a higher potential than that of the metal/semiconductor interface, causing an increase in the observed Schottky barrier height with respect to a large-area contact.

Nanoscale ohmic contacts

There are few reports describing the formation of nanoscale ohmic contacts partly because of the difficulty in the fabrication of an atomically flat, ohmic contact structure to a semiconductor layer. Any technique relying on diffusion to fabricate an ohmic contact to a semiconductor invariably causes non-uniform interfaces which preclude scaling to the nanometer length scale. There have been a few reports that an ohmic nanocontact to LTG:GaAs has been formed (Lee et al., 1999; 2000a) utilizing deposited metallic clusters without relying on diffusion techniques. In what follows, we will focus on this interesting development in more detail.

Ohmic nanocontact on GaAs

Substrate requirements

Electrical contacts for a nanometer scale device must provide low contact resistance and must be spatially uniform at the nanometer length scale. This requirement presents significant problems for nanocontacts based on any alloying process. For instance, in compound semiconductor devices based on GaAs, conventional contacts such as alloyed Au/Ge/Ni on n-type layers are spatially non-uniform and also consume a significant surface layer in order to provide suitably low specific contact resistivity (Baca et al., 1997). In this regard, uniform nonalloyed contacts are desired. Patkar et al. (1995) have reported that nonalloyed contacts employing LTG:GaAs surface layers can provide contact resistivities below $1 \times 10^{-6}\ \Omega{\cdot}\mathrm{cm}^2$. Since these contacts do not suffer from the deep interface and

spatially non-uniform alloying found in Au/Ge/Ni contacts, they are appropriate for nanometer scale device applications.

Fabrication

Nonalloyed ohmic nanocontact structures can be realized on a surface layer of LTG:GaAs. A controlled-geometry nanocontact is obtained by depositing a single crystal Au cluster (truncated octahedral shape) onto n-GaAs(100) having LTG:GaAs (undoped or Be-doped) based ohmic contact layers using *ex-situ* chemical self-assembly techniques. A self-assembled monolayer (SAM) of xylyl dithiol ($HS–CH_2–C_6H_4–CH_2–SH$, denoted as XYL) is first grown on the LTG:GaAs surface by soaking the sample in a 1 mM solution of XYL in acetonitrile for 12–18 h, followed by thorough rinsing in acetonitrile. This molecular layer forms an effective organic metal/semiconductor interface and provides both a robust mechanical tethering and a strong electronic coupling between the Au nanoclusters and the LTG:GaAs surface. A summary of the fabrication procedure can be found elsewhere (Lee et al., 1999). A schematic diagram of the resulting ohmic nanocontact structure is illustrated in Figure 6.

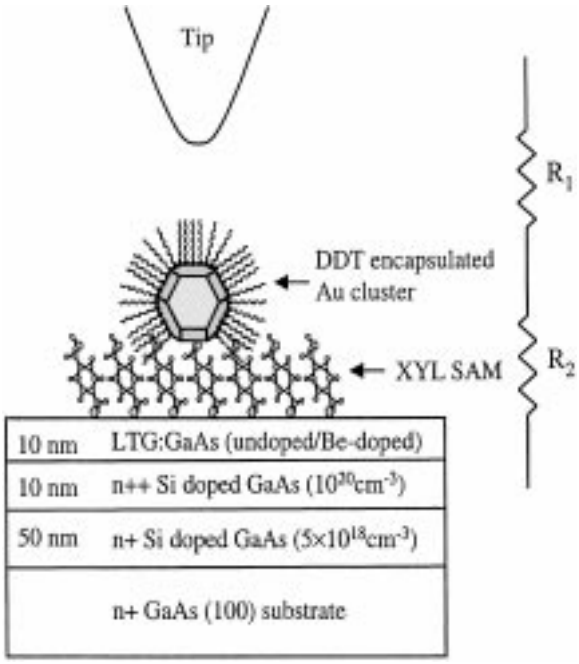

Figure 6. A schematic diagram of the nanocontact structure showing the GaAs epitaxial layers, the XYL monolayer, the deposited Au cluster encapsulated with DDT and STM tip. This system is modeled by two resistors connected in series. R_1 and R_2 are explained in text.

STM experimental data

After depositing Au clusters, the stability of the nanocontacts were checked by performing 100 consecutive images over an 80 min period of time. The Au clusters were observed to remain stable and did not exhibit any damage due to the scanning conditions employed. These observations indicate that the clusters are well tethered to the LTG:GaAs cap layer, in agreement with previous studies when Au clusters were well tethered by XYL molecules to a flat gold substrate (Dorogi et al., 1995; Andres et al., 1996a).

Figure 7 shows a series of representative measured STM $I–V$ data for cases where the STM tip was positioned over a Au cluster (solid curves C and D) and over the XYL-coated Be-doped LTG:GaAs surface (dashed curves A and B). The nearly linear $I–V$ obtained over the Au cluster implies that Au nanoclusters may be useful as nanometer-size ohmic contacts on GaAs. However, linear $I–V$ data by itself does not provide reliable information about the contact resistance R_2 of the cluster-to-semiconductor interface depicted in Figure 6. For example, if the contact resistance R_2 in Figure 6 is a low resistance ohmic contact, then the linear $I–V$ data is mainly due to R_1 since the $I–V$ measures the total resistance $R_{\text{total}} = R_1 + R_2$ and R_1 is typically much larger than R_2 in STM $I–V$ measurements in a low-current regime ($\sim$ nA range). In this case, only a small fraction of the applied voltage between tip and sample will be dropped across the contact interface (cluster-to-semiconductor) equal to the ratio of R_2/R_{total}. In order to increase this ratio and therefore make a significant contribution to the total voltage dropped across the contact interface, it is necessary to reduce R_1, which is done by bringing the STM tip close to Au cluster ('near contact mode STM').

The non-linear behavior $I–V$ over the substrate in Figure 7 (curves A and B) results because the STM tip probes the electronic states of XYL/LTG:GaAs. The non-linearity in $I–V$ on XYL/LTG:GaAs is due to the bandgap features of XYL and LTG:GaAs. It is similar to data obtained in studies on XYL/Au by STM, however in the latter case only XYL has this bandgap feature (Datta et al., 1997; Tian et al., 1998).

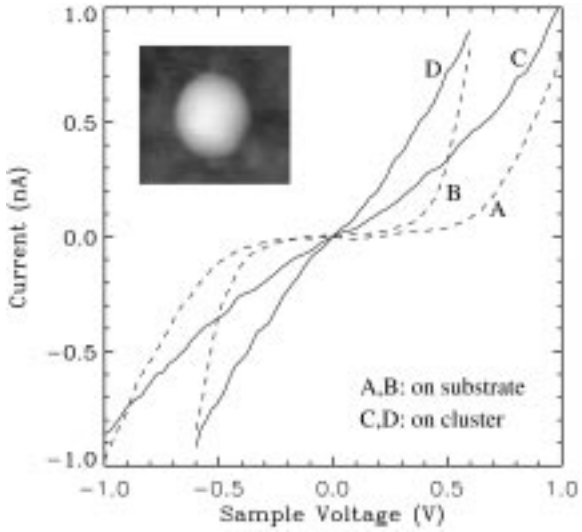

Figure 7. I–V data taken with the tip positioned over the XYL-coated substrate (dashed) and over a 4 nm diameter Au cluster (solid) with 0.8 nA for I_{set} and −1.0 V (A and C), −0.6 V (B and D) for V_{set}. Inset picture is a 20 nm × 20 nm UHV STM topographic image of the Au cluster tethered to the XYL-coated Be-doped LTG:GaAs, acquired with $I_{set} = 1.0$ nA and $V_{set} = -1.0$ V. (From Lee et al., 2000a.)

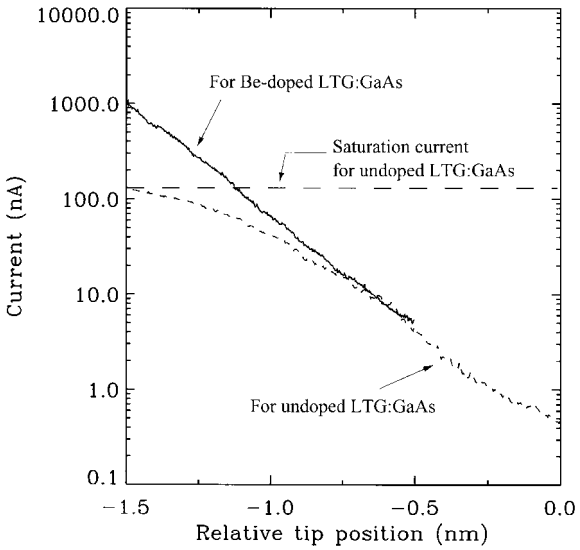

Figure 8. A log scale plot of I–z over a 4 nm diameter Au cluster, at constant $V_{set} = -1.0$ V for undoped LTG:GaAs cap layer (dotted) and for Be-doped cap layer (solid). The initial separation corresponding to $I_{set} = 0.5$ nA and 3.0 nA is plotted at zero and at −0.5 nm for undoped and Be-doped LTG:GaAs, respectively. (After Lee et al., 2000a.)

The ohmic behavior observed in Figure 7 (curves C and D) is found to persist in near contact mode STM I–V measurements when the tip is positioned over a Au cluster (Lee et al., 2000a). In this regime, a significant fraction of the applied voltage is dropped across the contact interface, permitting a useful estimate of its electronic properties.

The specific contact resistance (ρ_c) of this nanocontact can be estimated because well-characterized, single crystal Au nanoclusters were used in this study and these Au clusters orient with a hexagonal Au(111) facet parallel to the surface when deposited on an atomically flat substrate (Andres et al., 1996b). ρ_c is defined by R_2 and the contact area $\mathcal{A}$ under the Au cluster as

$$\rho_c = R_2 \times \mathcal{A}. \tag{1}$$

Since the STM measures R_{total}, the STM tip must be brought close to the cluster in order to estimate ρ_c and set realistic limits on the maximum current capability of the nanocontact. This is done by measuring current versus tip-cluster spacing (I–z) at a fixed bias (Lee et al., 1999). As the tip comes close to the cluster, R_1 is expected to become negligible, so the current will saturate at a value dictated by resistance R_2 which is the cluster–semiconductor substrate resistance of interest.

Figure 8 is a plot of I–z obtained with the tip positioned over a ∼4 nm diameter Au cluster on undoped LTG:GaAs (dotted line) and Be-doped LTG:GaAs (solid line) both of which have been passivated by an organic XYL layer. In this plot, the initial height of the tip above the cluster was set by specifying an I_{set} and V_{set}. Negative values for the relative tip position represent tip motion towards the sample. Data for the Be-doped sample were shifted by 0.5 nm to account for a difference in initial heights due to different set conditions. From geometrical considerations, the area $\mathcal{A}$ of a Au(111) facet on a ∼4 nm diameter, truncated octahedral cluster is $\sim 9 \times 10^{-14}$ cm^2. Therefore the ρ_c can be estimated from

$$\rho_c \simeq (V/I_{sat})\mathcal{A}, \tag{2}$$

where I_{sat} is saturation current at near contact. Current saturation as a function of tip motion in other STM experiments has also been observed on a metal surface (Gimzewski & Moller, 1987; Lang, 1987).

For the nanocontact on an undoped LTG:GaAs sample, a $\rho_c \simeq 1 \times 10^{-6}\ \Omega\cdot$cm^2 and a maximum current

density $J_{max} \simeq 1 \times 10^6$ A/cm^2 were determined using the saturation current (dashed horizontal line in Figure 8; 100 nA). Compared with undoped LTG:GaAs, a Be-doped LTG:GaAs cap layer (solid curve in Figure 8) did not show a saturation effect. Instead, the log scale I–z relationship remained roughly linear up to 1000 nA, the measurement limit of our system. This means that the tip is still not in close contact to the cluster surface. Using the maximum current (1000 nA) for the Be-doped LTG:GaAs capped sample, we determine an upper bound for ρ_c of $\simeq 1 \times 10^{-7}\ \Omega{\cdot}\text{cm}^2$ and a lower bound for J_{max} of $\simeq 1 \times 10^7\ A/cm^2$. The ohmic contact properties of nanocontact structures on undoped and Be-doped LTG:GaAs cap layer samples are summarized in Table 2.

Conduction model of ohmic nanocontact

A quantitative conduction model for a large-area ohmic contact (Ti/LTG:GaAs) has been recently developed (Chen et al., 2000). This analysis calculates the conduction band profiles for a given semiconductor structure by solving Poisson's equation, incorporating the characteristics of the LTG:GaAs defect states and Fermi statistics using parameters for the midgap defect states and shallow acceptor states in the LTG:GaAs material. This model adequately predicts the experimental trends (Patkar et al., 1995) for specific contact resistance (ρ_c) as a function of LTG:GaAs layer thickness and temperature.

Theoretical estimates for ρ_c can be calculated from a standard current density versus voltage (J–V) relationship

$$J = \frac{2e}{h}\int_0^\infty dE \int \frac{dk_\parallel}{(2\pi)^2} \times [f(-eV + E) - f(E)]\, T(E, k_\parallel), \qquad (3)$$

which is widely used in mesoscopic physics (Tian et al., 1998). In Eq. (3), $E = E_z + E_\parallel$, where z and $\parallel$ are the normal and parallel directions to the metal–semiconductor interface, respectively, f is the Fermi–Dirac distribution function, and T is the transmission probability function. The relevant physics of the problem is contained in realistically estimating T, especially for the case when the detailed nature of the XYL molecular tether is considered.

The XYL molecule is known to have a HOMO–LUMO gap (HOMO: highest occupied molecular orbital, LUMO: lowest unoccupied molecular orbital) of roughly 4 eV. In the gas phase, the HOMO and LUMO states are sharp and a negligible density-of-states (DOS) is present in the HOMO–LUMO gap. When bonded to Au(111), the HOMO and LUMO levels broaden considerably, resulting in a finite DOS in the gap region (Datta et al., 1997; Tian et al., 1998).

Three models were considered to estimate T for the nanocontact shown in Figure 9. From this study, the

Table 2. Summary of contact properties of the nanocontacts using undoped and Be-doped LTG:GaAs layer

	Nanocontact using undoped LTG:GaAs	Nanocontact using Be-doped LTG:GaAs
Saturation current	~ 100 nA	> 1000 nA
ρ_c	$\sim 1 \times 10^{-6}\ \Omega{\cdot}\text{cm}^2$	$\sim 1 \times 10^{-7}\ \Omega{\cdot}\text{cm}^2$
J_{max}	$\sim 1 \times 10^6$ A/cm^2	$\sim 1 \times 10^7$ A/cm^2

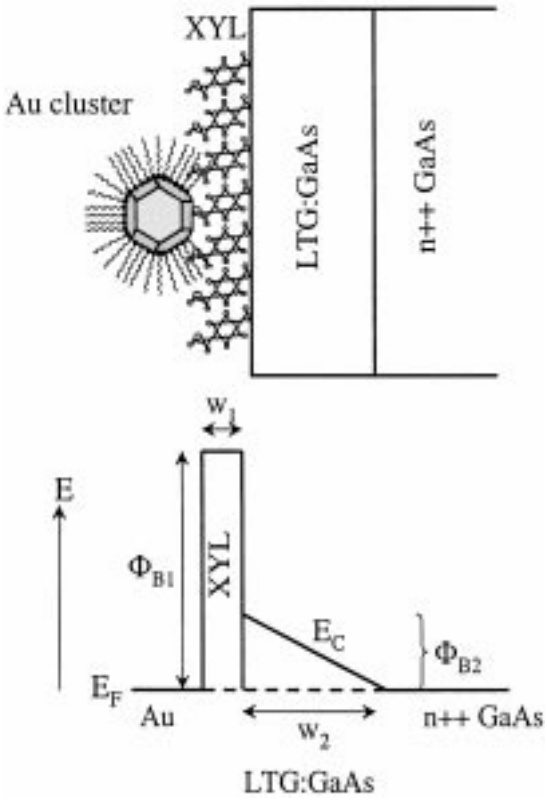

Figure 9. Nanocontact structure and the appropriate energy band diagram.

ohmic contact conduction mechanism is thought to arise primarily from the tunneling of electrons from the Au nanocluster into the GaAs layer with conduction through the midgap band of defect states in the LTG:GaAs layer playing an important role.

The first model (Model I in Figure 10) approximated the nanocontact as two tunnel barriers, one due to a rectangular barrier as a simple approximation to the XYL molecule and the other due to the depletion layer which forms at the LTG:GaAs interface. A WKB calculation of T (Simmons, 1963) through this barrier for realistic values of barrier width $w_1 = 0.9\,\text{nm}$ (XYL length), barrier height $\Phi_{B1} = 2\,\text{eV}$ (about one-half of HOMO–LUMO gap), $w_2 = 5$–$10\,\text{nm}$, and $\Phi_{B2} = 0.3$–$0.4\,\text{eV}$ yielded estimates of $\rho_c \simeq 10^{-1}\,\Omega{\cdot}\text{cm}^2$, a result that is about five orders of magnitude larger than measured experimentally ($\rho_c \simeq 10^{-6}\,\Omega{\cdot}\text{cm}^2$).

The second model (Model II in Figure 10) treated the XYL layer as a leaky dielectric, and not as an insulating barrier which would have zero DOS within the barrier. The finite DOS leads to a higher transmission probability, significantly enhancing the transport as compared with a perfectly insulating barrier between the cluster and the LTG:GaAs. Using this model, an estimate of $\rho_c \simeq 10^{-5}\,\Omega{\cdot}\text{cm}^2$ was obtained, providing better agreement with experiment than Model I.

The third model (Model III in Figure 10) provided the best overall agreement to experimental data. In this model, in addition to correctly treating transmission through the XYL molecule, the finite DOS introduced by the LTG:GaAs layer was taken into account, resulting in a sequential tunneling picture as shown in Figure 10. The DOS for the midgap states in the XYL–LTG:GaAs interface and the DOS in the n++ GaAs layer within a few $k_B T$ around the Fermi level are calculated to be $\sim 5 \times 10^{18}$ and $\sim 1 \times 10^{18}\,\text{cm}^{-3}$, respectively, which are comparable to each other. Therefore, electrons passing though the Au nanocluster into the LTG:GaAs first tunnel through the XYL barrier, are assisted by the large density of midgap states at the Fermi level which reside at the XYL–LTG:GaAs interface, and then tunnel through the LTG:GaAs barrier into the n++ GaAs layer. This sequential tunneling mechanism provides estimates of $\rho_c \simeq 10^{-6}\,\Omega{\cdot}\text{cm}^2$, providing excellent agreement with experiment. Detail calculations for all three models are given elsewhere (Lee, 2000b).

An example of the fit to the experimental data obtained using Model III and adjusting w_1, w_2, Φ_{B1}, and

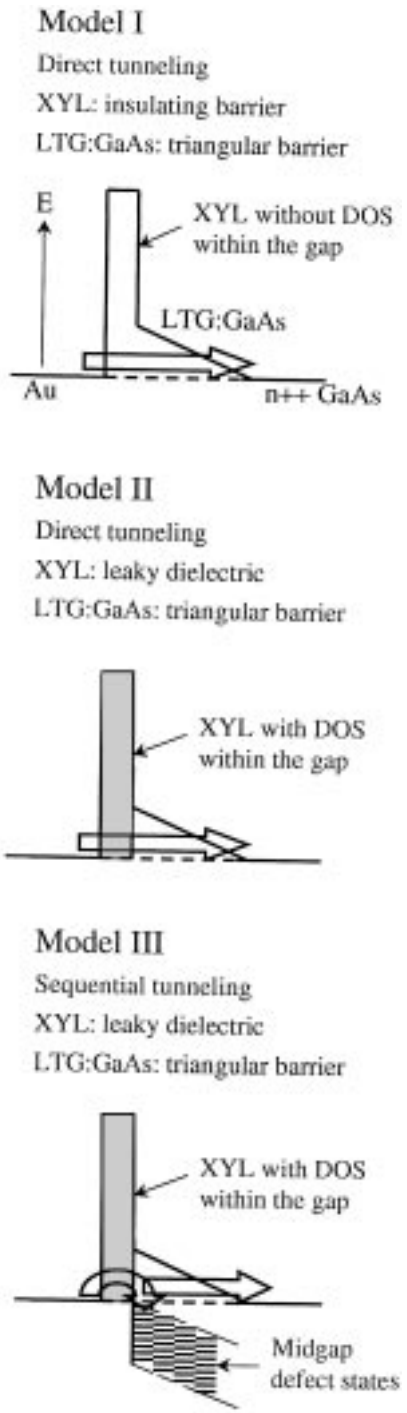

Figure 10. Schematic diagram illustrating three conduction models for the ohmic nanocontact structure.

the contact area is given in Figure 11 which shows a plot of the calculated current density versus voltage (J–V) (solid) for the nanocontact structure on an undoped LTG:GaAs capped sample. For comparison, the measured J–V is given as + symbols in the plot. As shown in Figure 11, the calculated and measured J–V curves are in a good agreement, suggesting that a sequential tunneling mechanism is the appropriate conduction model. In this plot, the voltage is the applied sample bias, therefore the J–V represents the reverse-bias region in a metal/semiconductor contact structure.

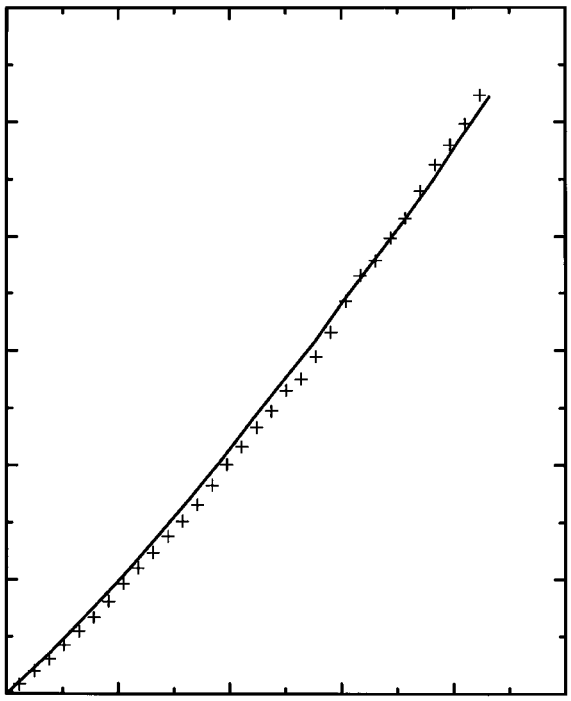

Figure 11. Calculated J–V (solid) and measured J–V (+ symbols) for a Au cluster nanocontact on an undoped LTG:GaAs capped sample. The voltage axis is the positive bias applied to the sample and corresponds to the reverse-bias region in metal/semiconductor interface.

Arrays of nanoclusters on semiconductor substrates

Chemical self-assembly can be used to fabricate hexagonal close-packed monolayers of nanoscale clusters on a semiconductor surface. This nanoscale ordering of individual nanoclusters can be further combined with a procedure which imposes a larger-scale pattern to break the symmetry of the uniform ordered self-assembled elements in controlled ways, imposing arbitrarily engineered patterns which provide non-uniform interconnections and directionality.

Unpatterned self-assembly

A simple method of forming monolayer arrays of Au nanoclusters is to spread a few drops of a colloidal solution containing nanoclusters on a flat solid substrate. As the solvent evaporates, the nanoclusters spontaneously organize into close-packed arrays. There are many examples of Au nanoclusters arrays studied by STM that have been fabricated on a variety of substrates, but in many cases, the arrays were not formed on semiconductors. Examples include unpatterned Au nanocluster arrays fabricated on MoS_2 (Andres et al., 1996b), on Au substrates (Houbertz et al., 1994; Bigioni et al., 1999), and on graphite substrates (Durston et al., 1997). Table 3 summarizes published results of array structures produced

Table 3. Summary of studies for fabrication of metallic nanoclusters arrays on semiconductors

Substrate (Thick, Solid)	Metallic cluster	Deposition environment	Patterning	Ordering	Characterization environment	Reference
MoS_2	Au ∼ 4 nm	*ex-situ*	Unpatterned	2-D ordered	TEM	Andres et al., 1996b
Au	Au ∼ 1 nm	*ex-situ*	Unpatterned	2-D non-ordered	UHV STM	Houbertz et al., 1994
Au	Au ∼ 2 nm	*ex-situ*	Unpatterned	2-D ordered	UHV STM	Bigioni et al., 1999
Graphite	Au ∼ 1 nm	*ex-situ*	Unpatterned	2-D ordered	UHV STM	Durston et al., 1997
Si	Au ∼ 2.6 nm	*ex-situ*	Patterned	2-D non-ordered	SEM	Vossmeyer et al., 1997
SiO_2/Si	Au ∼ 2 nm	*ex-situ*	Patterned	2-D non-ordered	SEM	Sato et al., 1997
SiO_2/Si	Au ∼ 2 nm	*ex-situ*	Patterned	2-D non-ordered	AFM	Parker et al., 1999
Si_3N_4	Au ∼ 1 nm	*ex-situ*	Patterned	2-D non-ordered	SEM & TEM	Clarke et al., 1997
GaAs	As ∼ 16 nm	*in-situ*	Patterned	1-D non-ordered	TEM	Hung et al., 1999
GaAs	Au ∼ 5 nm	*ex-situ*	Patterned	2-D ordered	SEM & UHV STM	Liu et al., 2000

by the self-assembly of nanoscale metallic clusters on thick solid substrates.

Only a few examples of self-assembled cluster arrays on semiconductors have been reported. The drop casting method, although it is easy to implement, cannot be used to fabricate large-area, well-ordered arrays. To form a large-area, well-ordered monolayer array of Au nanoclusters, a different technique was developed (Liu et al., 2000). A colloidal solution of dodecanethiol (DDT) encapsulated Au clusters in hexane was spread over a water surface. Upon solvent evaporation, the Au nanoclusters spontaneously organized into a hexagonal close-packed monolayer array at the air/water interface. This monolayer was then transferred onto the semiconductor substrate by gently touching it with the substrate.

In order to verify the local and long-range ordering of the cluster arrays, the arrays were also transferred to an amorphous carbon film supported on a copper grid. A TEM micrograph of such a monolayer array is shown in Figure 12. It reveals a highly ordered, hexagonal close-packed array of Au nanoclusters. The relative orientation of the clusters in this array is preserved over microns, with a cluster vacancy density of $\sim 10^{-4}$ times the cluster density ($\sim 2 \times 10^{12}$ clusters/cm^2). The Au nanoclusters in Figure 12 have a mean diameter of 5.2 ± 0.6 nm and an average edge-to-edge spacing of 3.1 ± 0.2 nm. This spacing between neighboring clusters is close to twice the length of DDT molecule (~ 1.6 nm), indicating that the DDT molecules surrounding each Au nanocluster are nearly fully extended.

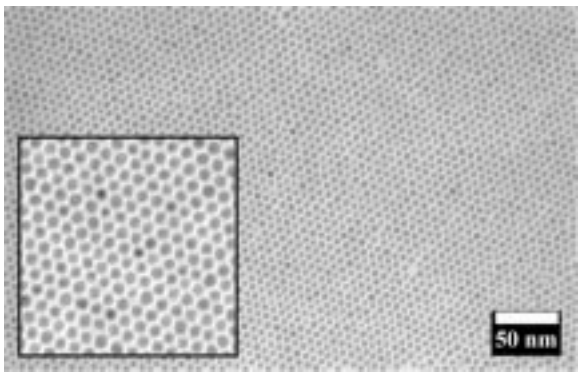

Figure 12. A TEM micrograph of a hexagonal close-packed monolayer of DDT encapsulated Au nanoclusters transferred from a water surface to a carbon TEM grid. The inset is a 100 nm × 100 nm enlarged view of the cluster array. (From Liu et al., 2000.)

Au nanocluster monolayer arrays similar to the array shown in Figure 12 were transferred onto a LTG:GaAs semiconductor substrate previously coated with a SAM of the XYL tether molecule. GaAs with a Be-doped LTG:GaAs surface layer was used for the substrate (see Figure 6). Figure 13 is a UHV STM image of the Au nanocluster arrays transferred from a water surface to an XYL-coated Be-doped LTG:GaAs substrate. A well-ordered hexagonal close-packed structure was observed. This image indicates that the interface layer of XYL provides a robust mechanical tethering of the Au nanoclusters to the LTG:GaAs surface and electronically links the Au clusters to the LTG:GaAs surface via the nanocontact mechanism described above. The center-to-center distance between neighboring clusters was determined to be 7.9 ± 0.6 nm, a result consistent with that obtained from a parallel TEM study (~ 8.3 nm) (see Figure 12). The highly ordered array extended over $\sim 0.1\mu$m, which is the maximum scan size of the UHV STM.

Representative I–V curves obtained for the sample shown in Figure 13 are shown in Figure 14, for the case where the STM tip is directly over three cluster sites (solid curves A) and for the case where the STM tip is positioned between clusters (dashed curve B). As was observed in previous experiments with isolated clusters

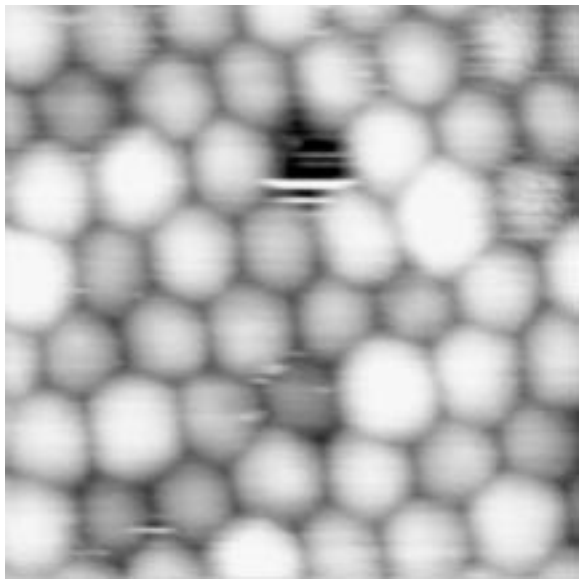

Figure 13. A 50 nm × 50 nm UHV STM topographic image of close-packed 2-D array of Au nanoclusters tethered to the XYL-coated Be-doped LTG:GaAs, acquired with $V_{set} = -1.2$ V and $I_{set} = 0.1$ nA. There is a defect site (vacancy) in this image.

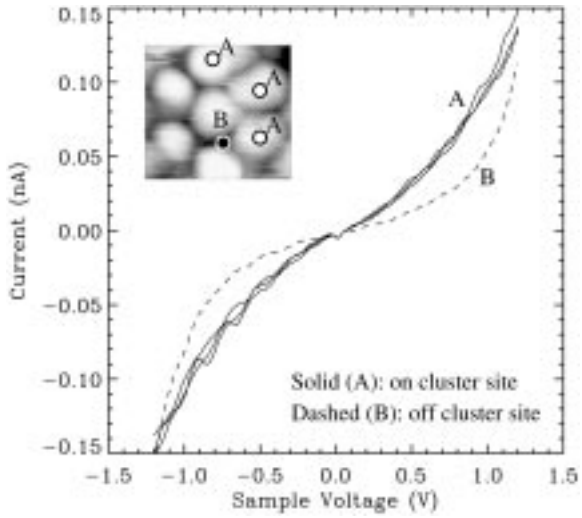

Figure 14. I–V data taken with the STM tip positioned over on-cluster sites (solid curves A) and over an off-cluster site (dashed curve B) with $I_{set} = 0.15$ nA and $V_{set} = -1.2$ V. Inset picture is a 25 nm × 25 nm UHV STM image of array of Au clusters tethered to XYL-coated Be-doped LTG:GaAs, acquired with $I_{set} = 0.1$ nA and $V_{set} = -1.2$ V.

(Lee et al., 2000a), a reasonably linear I–V is observed when the tip is positioned over a cluster. The difference in shape of the I–V curve between the tip 'on' and 'off' a cluster site is not as dramatic for the case of an array as for the case of an isolated cluster. It is likely that there is some conduction through adjacent clusters in the 'off-cluster' case due to the finite end form of the tip which was estimated to be 10–15 nm in diameter from a separate TEM study.

The cluster array used in this study is 'unlinked', i.e. adjacent clusters within this array are separated by the DDT encapsulant and not linked by conductive molecules such as XYL. In this case, the coupling to the semiconductor substrate is much stronger than the intercluster coupling. It has been shown to be possible to control the cluster-to-cluster resistance within an array of Au nanoclusters by exposing the array to a solution containing a linking molecule (Andres et al., 1996b). It should therefore be possible to change the relative strength of the intercluster electronic coupling with respect to the coupling to the semiconductor device layers. If the intercluster coupling is made much stronger than the cluster-to-semiconductor coupling, the resulting patterned array structure represents an interesting interconnect structure which has been termed a 'molecular ribbon' (Datta et al., 1998).

Patterned self-assembly

Realistic nanoelectronic device applications require a precise control in positioning of the nanoscale clusters on a semiconductor substrate. Several methods have been proposed to realize this spatial positioning.

As summarized in Table 3, Vossmeyer et al., used a light-directed, selective deposition technique to produce patterning of passivated Au nanoclusters (2.6 nm in diameter) onto a Si substrate (Vossmeyer et al., 1997). Another approach using electron-beam lithography or photolithography lift-off techniques yielded results that are shown in Figure 15. Following this approach, Au nanoclusters were selectively deposited on pre-patterned regions on a SiO_2/Si substrate (Sato et al., 1997; Parker et al., 1999) and a Si_3N_4 substrate (Clarke et al., 1997). Following yet another approach, Hung et al., used crystal strain to direct assembly of nanoparticles (arsenic precipitates; ∼ 16 nm in diameter) within GaAs-based epitaxial layers grown at low temperature by MBE (Hung et al., 1999). They observed 1-D arrays of arsenic nanoparticles in these LTG:GaAs-based layers. However, these prior studies have not realized well-ordered structures such as close-packed arrays of nanoclusters nor have they shown strong electronic coupling between the nanoclusters and the semiconductor.

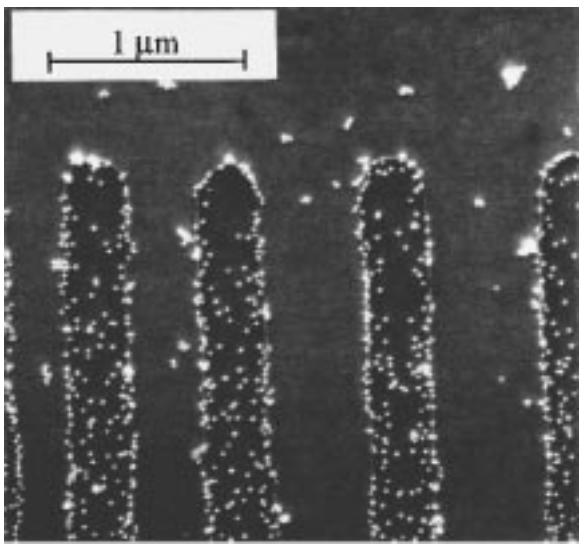

Figure 15. An SEM micrograph showing an example of patterned, 20 nm Au colloidal particles on SiO_2/Si. (From Sato et al., 1997.)

Toward this purpose, a combination of soft lithography using microcontact printing and directed self-assembly has been developed to produce patterned arrays of Au nanoclusters (Liu et al., 2000). A prefabricated pattern of tethering molecules is first transferred to the semiconductor surface using microcontact printing (Kumar & Whitesides, 1993; Xia & Whitesides, 1998). Then a large-area close-packed array of Au nanoclusters is transferred to the substrate using the process described in the previous section. Finally, a solvent rinse is used to remove nanoclusters from the regions not coated with the tether molecule.

In particular, a SAM of XYL was deposited in predefined regions on a LTG:GaAs substrate using microcontact printing. This serves as a tether template for Au nanoclusters. Previous studies have shown that SAMs of alkanethiols can be used as electron-beam photoresists on GaAs with resolutions below 10 nm (Lercel et al., 1996). In the current study, double-ended XYL was selected to provide the patterned tether. Conventional photoresist based techniques are generally not suitable for directing the self-assembly due to the associated nonplanarity of the surfaces, potential for molecular level contamination, and the possibility of interactions between the chemicals used in the photoresist processing and the self-assembly deposition.

A patterned array of Au nanoclusters on LTG:GaAs fabricated by this technique was imaged using a SEM, as shown in Figure 16(a). In this image, the light regions are the bare LTG:GaAs substrate and the dark regions are covered by Au nanocluster arrays. Although the SEM cannot resolve individual clusters, the contrast between the two types of regions indicates that the use of patterned tether regions has resulted in deposition of Au nanocluster arrays primarily within the selected regions. The lines and cells illustrated in this pattern represent two important structures for defining computational structures and the interconnections between such cells. The width of the patterned lines are $\sim 3\mu$, but both the stamp pad patterning of XYL tether molecule and the deposition of nanocluster arrays on the surface should be applicable to patterns with deep submicron dimensions.

The short-range order in the cluster covered regions was investigated using UHV STM as shown in Figure 16(b). In images obtained with smaller scan sizes, the hexagonal facets of individual Au clusters were clearly visible. The well-defined, stable STM images verify that ordered arrays were transferred to the XYL-coated regions on the LTG:GaAs surface and that the clusters are well tethered mechanically and electronically to the surface. By introducing conducting molecules between patterned Au clusters, the resulting patterned array structure might posses interesting interconnect possibilities.

Conclusions

Research on the electronic properties of metallic nanoclusters deposited on semiconductor substrates have been summarized. These structures are of potential

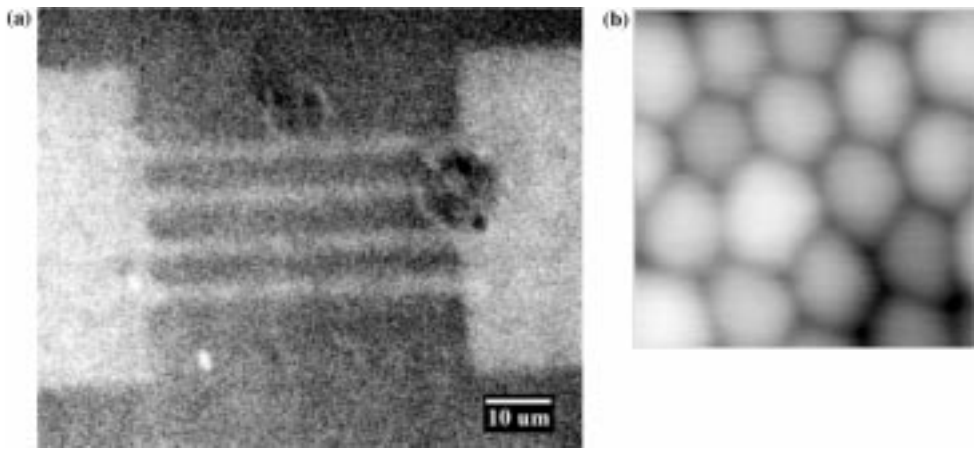

Figure 16. (a) An SEM micrograph of a patterned Au nanocluster array on LTG:GaAs. The light colored regions are bare LTG:GaAs and the dark colored areas are regions covered by Au nanoclusters. (b) A 30 nm × 30 nm UHV STM topographic image of the Au nanoclusters in the XYL defined regions on the LTG:GaAs substrate, acquired with $I_{set} = 200$ pA and $V_{set} = -1.5$ V. (From Liu et al., 2000.)

interest for nanoelectronic device applications. Current efforts in this area are focussed on nanometer-scale single-electron devices, Schottky diodes, and ohmic nanocontacts. Efforts to pattern these nanoclusters in pre-defined ways on semiconductor substrates have also been reviewed. The reported results may well form a viable technique for high throughput fabrication of future nanoelectronic devices.

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References

Andres R.P., T. Bein, M. Dorogi, S. Feng, J.I. Henderson, C.P. Kubiak, W. Mahoney, R.G. Osifchin & R. Reifenberger, 1996a. Coulomb staircase at room temperature in a self-assembled molecular nanostructure. Science 272, 1323–1325.

Andres R.P., J.D. Bielefeld, J.I. Henderson, D.B. Janes, V.R. Kolagunta, C.P. Kubiak, W.J. Mahoney & R.G. Osifchin, 1996b. Self-assembly of a two-dimensional superlattice of molecularly linked metal clusters. Science 273, 1690–1693.

Baca A.G., F. Ren, J.C. Zopler, R.D. Briggs & S.J. Pearton, 1997. A survey of ohmic contacts to III–V compound semiconductor. Thin Solid Films 308–309, 599–606.

Bandyopadhyay S. & V.P. Roychowdhury, 1996. Computational paradigms in nanoelectronics: Quantum coupled single electron logic and neuromorphic networks. Jpn. J. Appl. Phys. 35, 3350–3362.

Bigioni P.P., L.E. Harrell, W.G. Cullen, D.K. Guthrie, R.L. Whetten & P.N. First, 1999. Imaging and tunneling spectroscopy of gold nanoclusters and nanocrystal arrays. Eur. Phys. J. D6, 355–364.

Binnig G., H. Rohrer, Ch. Gerber & E. Weibel, 1982. Surface studies by scanning tunneling microscopy. Phys. Rev. Lett. 49, 57–61.

Bowles R.S., J.J. Kolstad, J.M. Calo & R.P. Andres, 1981. Generation of molecular clusters of controlled size. Surf. Sci. 106, 117–124.

Brillson L.J., R.E. Viturro, C. Mailhiot, J.L. Shaw, N. Tache, J. McKinley, G. Margaritondo, J.M. Woodall, P.D. Kirchner, G.D. Pettit & S.L. Wright, 1988. Unpinned schottky barrier formation at metal-GaAs interfaces. J. Vac. Sci. Technol. B6, 1263–1269.

Brune H., M. Giovannini, K. Bromann & K. Kern, 1998. Self-organized growth of nanostructure arrays on strain–relief patterns. Nature 394, 451–453.

Brust M., M. Walker, D. Bethell, D.J. Schiffrin & R. Whyman, 1994. Synthesis of thiol-derivatised gold nanoparticles in a two-phase liquid–liquid. J. Chem. Soc. Chem. Commun. 1994, 801–802.

Carroll D.L., M. Wagner, M. Rühle & D.A. Bonnell, 1997. Schottky-barrier formation at nanoscale metal–oxide interfaces. Phys. Rev. B55, 9792–9799.

Chao L.C. & R.P. Andres, 1994. Synthesis of a supported metal catalyst using nanometer-size clusters. J. Colloid Interface Sci. 165, 290–295.

Chen N.-P., H.J. Ueng, D.B. Janes, J.M. Woodall & M.R. Melloch, 2000. A quantitative conduction model for a low-resistance nonalloyed ohmic contact structure utilizing low-temperature-grown GaAs. J. Appl. Phys. 88, 309–315.

Choi E. & R.P. Andres, 1987. Isolation of monodispersed gold clusters of controlled size. In: Jena P., Rao B.K. & Khanna S.N. eds. Physics and Chemistry of Small Clusters. NATO ASI Series B. Vol. 158. Plenum Press, New York, pp. 61–65.

Chung S.-W., G. Markovich & J.R. Heath, 1998. Fabrication and alignment of wires in two dimensions. J. Phys. Chem. B 102, 6685–6687.

Clarke L., M.N. Wybourne, M. Yan, S.X. Cai, L.O. Brown, J. Hutchison, & J.F.W. Keana, 1997. Fabrication and near-room temperature transport of patterned gold cluster structures. J. Vac. Sci. Technol. B 15, 2925–2929.

Crommie M.F., C.P. Lutz & D.M. Eigler, 1993. Confinement of electrons to quantum corrals on a metal surface. Science 262, 218–220.

Dai H., N. Franklin & J. Han, 1998. Exploiting the properties of carbon nanotubes for nanolithography. Appl. Phys. Lett. 73, 1508–1510.

Datta S., W. Tian, S. Hong, R. Reifenberger, J.I. Henderson & C.P. Kubiak, 1997. Current-voltage characteristics of self-assembled monolayers by scanning tunneling microscopy. Phys. Rev. Lett. 79, 2530–2533.

Datta S., D.B. Janes, R.P. Andres, C.P. Kubiak & R. Reifenberger, 1998. Molecular ribbons. Semicond. Sci. Tech. 13, 1347–1353.

Dorogi M., J. Gomez, R. Oschifin, R.P. Andres & R. Reifenberger, 1995. Room-temperature Coulomb blockade from a self-assembled molecular nanostructure. Phys. Rev. B52, 9071–9077.

Durston P.J., J. Schmidt, R.E. Palmer & J.P. Wilcoxon, 1997. Scanning tunneling microscopy of ordered coated cluster layers on graphite. Appl. Phys. Lett. 71, 2940–2942.

Eigler D.M. & E.K. Schweizer, 1990. Positioning single atoms with a scanning tunnelling microscope. Nature 344, 524–526.

Fan S., M.G. Chapline, N.R. Franklin, T.W. Tombler, A.M. Cassell & H. Dai, 1999. Self-oriented regular arrays of carbon nanotubes and their field emission properties. Science 283, 512–514.

First P.N., J.A. Stroscio, R.A. Dragoset, D.T. Pierce & R.J. Celotta, 1989. Metallicity and gap states in tunneling to Fe clusters on GaAs(110). Phys. Rev. Lett. 63, 1416–1419.

Gheber L.A., G. Gorodetsky & V. Volterra, 1994. Studies of submicron gold islands on silicon by STM. Thin Solid Films 238, 1–3.

Gimzewski J.K. & R. Möller, 1987. Transition from the tunneling regime to point contact studied using scanning tunneling microscopy. Phys. Rev. B36, 1284–1287.

Hasegawa H., T. Sato & C. Kaneshiro, 1999. Properties of nanometer-sized metal-semiconductor interfaces of GaAs and InP formed by an *in situ* electrochemical process. J. Vac. Sci. Technol. B 17, 1856–1866.

Heine V., 1965. Theory of surface states. Phys. Rev. 138, A1689–A1696.

Hong S., D.B. Janes, D. McInturff, R. Reifenberger & J.M. Woodall, 1996. Stability of a low-temperature grown GaAs surface layer following air exposure using tunneling spectroscopy. Appl. Phys. Lett. 68, 2258–2260.

Hong S., J. Zhu & C.A. Mirkin, 1999. Multiple ink nanolithography: toward a multiple-pen nano-plotter. Science 286, 523–525.

Houbertz R., T. Feignspan, F. Mielke, U. Memmert, U. Hartmann, U. Simon, G. Schon & G. Schmid, 1994. STM investigation on compact Au_{55} cluster pellets. Europhys. Lett. 28, 641–646.

Hu X., D. Sarid & P. von Blanckenhagen, 1999. Nano-patterning and single electron tunneling using STM. Nanotechnology 10, 209–212.

Hung C.-Y., A.F. Marshall, D.-K. Kim, W.D. Nix, J.S. Harris Jr & R.A. Kiehl, 1999. Strain directed assembly of nanoparticle arrays within a semiconductor. J. Nanoparticle Research 1, 329–347.

Jiang C.-S., T. Nakayama & M. Aono, 1999. Spatially resolved observation of Coulomb blockade and negative differential conductance on a Ag cluster on the clean GaAs(110) surface. Appl. Phys. Lett. 74, 1716–1718.

Johnson K.S., J.H. Thywissen, N.H. Dekker, K.K. Berggren, A.P. Chu, R. Younkin & M. Prentiss, 1998. Localization of metastable atom beams with optical standing waves: Nanolithography at the Heisenberg limit. Science 280, 1583–1586.

Kiely C.J., J. Fink, M. Brust, D. Bethell & D.J. Schiffrin, 1998. Spontaneous ordering of bimodal ensembles of nanoscopic gold clusters. Nature 396, 444–446.

Korgel B.A. & D. Fitzmaurice, 1998. Self-assembly of silver nanocrystals into two-dimensional nanowire arrays. Adv. Mater. 10, 661–665.

Kumar A. & G.M. Whitesides, 1993. Features of gold having micrometer to centimeter dimensions can be formed through a combination of stamping with an elastomeric stamp and an alkanethiol 'ink' followed by chemical etching. Appl. Phys. Lett. 63, 2002–2004.

Lang N.D., 1987. Resistance of a one-atom contact in the scanning tunneling microscope. Phys. Rev. B36, 8173–8176.

Lee T., J. Liu, D.B. Janes, V.R. Kolagunta, J. Dicke, R.P. Andres, J. Lauterbach, M.R. Melloch, D. McInturff, J.M. Woodall & R. Reifenberger, 1999. An ohmic nanocontact to GaAs. Appl. Phys. Lett. 74, 2869–2871.

Lee T., N.-P. Chen, J. Liu, R.P. Andres, D.B. Janes, E.H. Chen, M.R. Melloch, J.M. Woodall & R. Reifenberger, 2000a. Ohmic nanocontacts to GaAs using undoped and p-doped layers of low-temperature-grown GaAs, Appl. Phys. Lett. 76, 212–214.

Lee T., 2000b, Electronic properties of Au nanoclusters/semiconductor structures with low resistance interfaces. Ph.D. thesis, Purdue University.

Lercel M.J., H.G. Craighead & D.L. Allara, 1996. Sub-10 nm lithography with self-assembled monolayers. Appl. Phys. Lett. 68, 1504–1506.

Liu J., T. Lee, D.B. Janes, B.L. Walsh, M.R. Melloch, J.M. Woodall, R. Reifenberger & R.P. Andres, 2000. Guided self-assembly of Au nanocluster arrays electronically coupled to semiconductor device layers. Appl. Phys. Lett. 77 (in press).

Louie S.G., & M.L. Cohen, 1976. Electronic structure of metal-semiconductor interface. Phys. Rev. B13, 2461–2469.

Melloch M.R., J.M. Woodall, E.S. Harmon, N. Otsuka, F.H. Pollak, D.D. Nolte, R.M. Feenstra & M.A. Lutz, 1995. Low-temperature grown III-V materials. Annu. Rev. Mater. Sci. 25, 547–600.

Monch W., 1999. Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities. J. Vac. Sci. Technol. B 17, 1867–1876.

Murray C.B., C.R. Kagan & M.G. Bawendi, 1995. Self-organization of CdSe nanocrystallites into three-dimensional quantum dot superlattices. Science 270, 1335–1338.

Nalwa H.S. (ed.), 2000. Handbook of Nanostructured Materials and Nanotechnology, Vol. 1–5. Academic Press, San Diego, USA.

Ng T.-B., D.B. Janes, D. McInturff & J.M. Woodall, 1996. Inhibited oxidation in low-temperature grown GaAs surface layers observed by photoelectron spectroscopy. Appl. Phys. Lett. 69, 3551–3553.

Park K.-H., M. Shin, J.S. Ha, W.S. Yun & Y.-J. Ko, 1999. Fabrication of lateral single-electron tunneling structures by field-induced manipulation of Ag nanoclusters on a silicon surface. Appl. Phys. Lett. 75, 139–141.

Parker A.J., P.A. Childs, R.E. Palmer & M. Brust, 1999. Deposition of passivated gold nanoclusters onto prepatterned substrates. Appl. Phys. Lett. 74, 2833–2835.

Patkar M.P., T.P. Chin, J.M. Woodall, M.S. Lundstrom & M.R. Melloch, 1995. Very low resistance nonalloyed ohmic contacts using low-temperature molecular beam epitaxy of GaAs. Appl. Phys. Lett. 66, 1412–1414.

Radojkovic P., M. Schwartzkopff, M. Enachescu, E. Stefanov, E. Hartmann & F. Koch, 1996. Observation of Coulomb staircase and negative differential resistance at room temperature by scanning tunneling microscopy. J. Vac. Sci. Technol. B 14, 1229–1233.

Roychowdhury V.P., D.B. Janes, S. Bandyopadhyay & X. Wang, 1996. Collective computational activity in self-assembled arrays of quantum dots: A novel neuromorphic architecture. IEEE Trans. Electr. Dev. 43, 1688–1699.

Sato T., D.G. Hasko & H. Ahmed, 1997. Nanoscale colloidal particles: Monolayer organization and patterning. J. Vac. Sci. Technol. B 15, 1–4.

Sato T., C. Kaneshiro, H. Okada & H. Hasegawa, 1999. Formation of size and position controlled nanometer size Pt dots on GaAs and InP substrates by pulsed electrochemical deposition. Jpn. J. Appl. Phys. Part. 1 38, 2448–2452.

Simmons J.G., 1963. Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film. J. Appl. Phys. 34, 1793–1803.

Snow A.W. & H. Wohltjen, 1998. Size-induced metal to semiconductor transition in a stabilized gold cluster ensemble. Chem. Mater. 10, 947–949.

Tersoff J., 1984. Schottky barrier heights and the continuum of gap states. Phys. Rev. Lett. 52, 465–468.

Tersoff J., 1988. In: Metallization and Metal–Semiconductor Interfaces. Proceedings of a NATO Advanced Research Workshop, Garching, West Germany, 1988. Plenum, New York, USA, 1989, 281–288.

Tian W., S. Datta, S. Hong, R. Reifenberger, J.I. Henderson & C.P. Kubiak, 1998. Conductance spectra of molecular wires. J. Chem. Phys. 109, 2874–2882.

Vossmeyer T., E. DeIonno & J.R. Heath, 1997. Light-directed assembly of nanoparticles. Angew. Chem. Int. Ed. Engl. 36, 1080–1083.

Whetten R.L., J.T. Khoury, M.M. Alvarez, S. Murthy, I. Vezmar, Z.L. Wang, P.W. Stephens, C.L. Cleveland, W.D. Luedtke & U. Landman, 1996. Nanocrystal gold molecules. Adv. Mater. 8, 428–433.

Wohltjen H. & A.W. Snow, 1998. Colloidal metal-insulator-metal ensemble chemresisitor sensor. Anal. Chem. 70, 2856–2859.

Woodall J.M. & J.L. Freeouf, 1981. GaAs metallization: Some problems and trends. J. Vac. Sci. Technol. 19, 794–798.

Xia Y. & G.M. Whitesides, 1998. Soft lithography. Angew. Chem. Int. Ed. 37, 550–575.

Correction

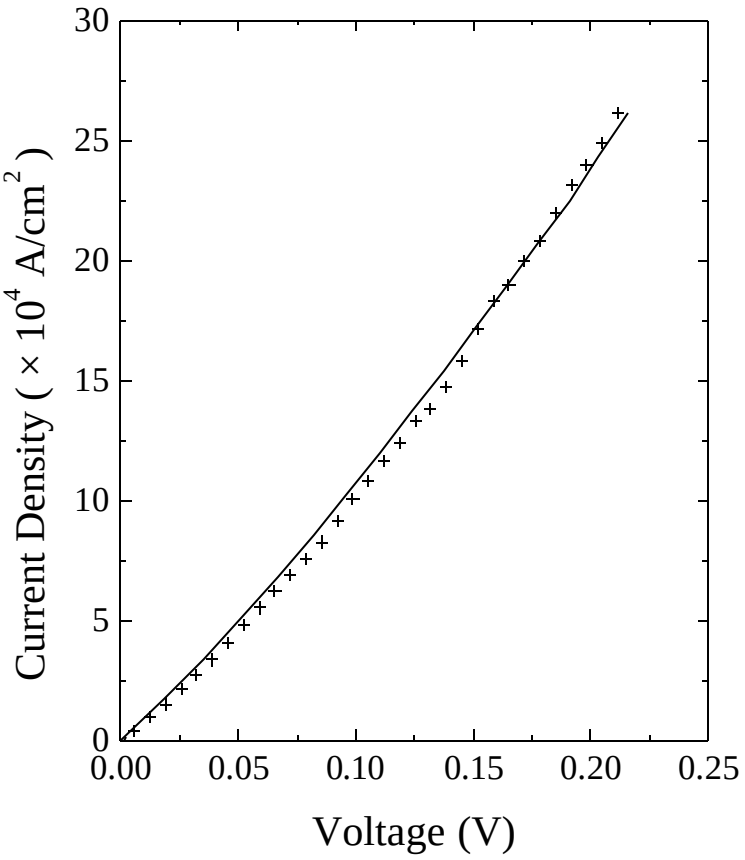

Figure 11. Calculated J –V (solid) and measured J –V (+ symbols) for a Au cluster nanocontact on an undoped LTG:GaAs capped sample. The voltage axis is the positive bias applied to the sample and corresponds to the reverse-bias region in metal/semiconductor interface.